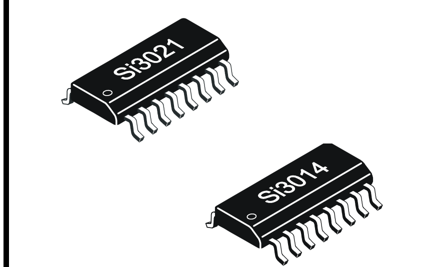
Si3034

3.3 V GLOBAL DIRECT ACCESS ARRANGEMENT

Features

Complete DAA includes the following:

- Programmable Line Interface
  - AC Termination
  - DC Termination
  - Ring Detect Threshold
  - Ringer Impedance
- 84 dB Dynamic Range TX/RX Paths
- Integrated Analog Front End (AFE) and 2- to 4-Wire Hybrid
- Integrated Ring Detector
- Caller ID Support
- Loop Current Monitor
- Clock Generation
- Pulse Dialing Support
- Billing Tone Detection
- Overload Detection
- Low Profile 16-Pin SOIC Packages
- 3.3 or 5 V Power Supply
- Direct Interface to DSPs
- Daisy-Chaining for Up to Eight Devices
- Greater than 3000 V Isolation
- Proprietary ISOcap™ Technology



Ordering Information

See page 61.

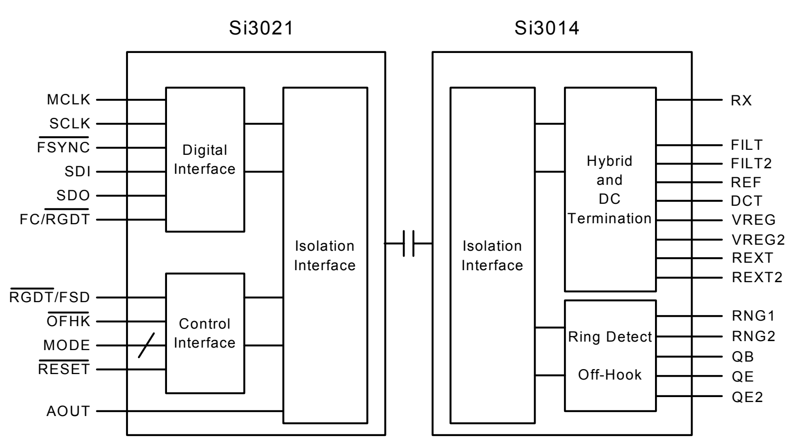
Applications

- V.90 Modems
- Voice Mail Systems
- Set Top Boxes
- Fax Machines

Description

The Si3034 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. Available in two 16-pin small outline packages, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3034 dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The Si3034 interfaces directly to standard modem DSPs.

Functional Block Diagram



Pin Assignments

Si3021 (SOIC)

MCLK	1	16	OFHK
FSYNC	2	15	RGDT/FSD
SCLK	3	14	M0
V_D	4	13	V_A
SDO	5	12	GND
SDI	6	11	C1A
FC/RGDT	7	10	M1
RESET	8	9	AOUT

Si3021 (TSSOP)

SDO	1	16	V_D
SDI	2	15	SCLK
FC/RGDT	3	14	FSYNC
RESET	4	13	MCLK
AOUT	5	12	OFHK
M1	6	11	RGDT/FSD
C1A	7	10	M0
GND	8	9	V_A

Si3014 (SOIC or TSSOP)

QE2	1	16	FILT2
DCT	2	15	FILT
IGND	3	14	RX
C1B	4	13	REXT
RNG1	5	12	REXT2
RNG2	6	11	REF
QB	7	10	VREG2
QE	8	9	VREG

US Patent # 5,870,046
US Patent # 6,061,009
Other Patents Pending

Table of Contents

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade	0	25	70	°C
Si3021 Supply Voltage, Analog	V_A		4.75	5.0	5.25	V
Si3021 Supply Voltage, Digital[3]	V_D		3.0	3.3/5.0	5.25	V

Notes:

1. The Si3034 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si3021 and any Si3014 are used. See Figure 16 on page 15 for typical application circuit.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, can operate from either 3.3 V or 5.0 V. The Si3021 supports interface to 3.3 V logic when operating from 3.3 V and applies to both the serial port and the digital signals $\overline{\text{RGDT}}$/FSD, $\overline{\text{OFHK}}$, $\overline{\text{RESET}}$, M0, and M1.

SILICON LABORATORIES

Table 2. Loop Characteristics
(V_D = 3.3 to 5.25 V, T_A = 0 to 70°C for K-Grade, See Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 1 DCT = 11 (CTR21)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 42 mA, ACT 1 DCT 11 (CTR21)	—	—	14.5	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ACT = 1 DCT = 11 (CTR21)	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ACT = 1 DCT = 11 (CTR21)	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 01 (Japan)	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 01 (Japan)	11	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 10 (FCC)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 10 (FCC)	12	—	—	V
On Hook Leakage Current	I_{LK}	V_{TR} = –48V	—	—	1	µA
Operating Loop Current	I_{LP}	FCC/Japan Modes	13	—	120	mA
Operating Loop Current	I_{LP}	CTR21 Mode	13	—	60	mA
DC Ring Current		w/o Caller ID	—	—	20	µA
DC Ring Current		with Caller ID	—	450	—	µA
Ring Detect Voltage[1]	V_{RD}	RT = 0	11	—	22	V_{RMS}
Ring Detect Voltage[1]	V_{RD}	RT = 1	17	—	33	V_{RMS}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number[2]	REN	w/o Caller ID	—	—	0.2	
Ringer Equivalence Number[2]	REN	with Caller ID	—	0.8	—	

Notes:
1. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
2. C15, R14, Z2, and Z3 not installed. See "Ringer Impedance," on page 24.

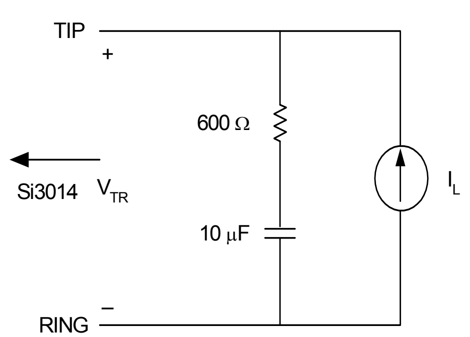


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 5 V

(V_D = 4.75 to 5.25 V, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		3.5	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	3.5	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[1]	I_D	V_D pin	—	14	18	mA
Total Supply Current, Sleep Mode[1]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.3	2.5	mA
Total Supply Current, Deep Sleep[1,2]	$I_A + I_D$	PDN = 1, PDL = 1	—	.04	0.5	mA

Notes:
1. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
2. $\overline{\text{RGDT}}$ is not functional in this state.

Table 4. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70°C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog[1,2]	I_A	V_A pin	—	0.3	1	mA
Power Supply Current, Digital[3]	I_D	V_D pin	—	9	12	mA
Total Supply Current, Sleep Mode[3]	$I_A + I_D$	PDN = 1, PDL = 0	—	1.2	2.5	mA
Total Supply Current, Deep Sleep[3,4]	$I_A + I_D$	PDN = 1, PDL = 1	—	.04	0.5	mA
Power Supply Voltage, Analog[1,5]	V_A	Charge Pump On	4.3	4.6	5.0	V

Notes:
1. Only a decoupling capacitor should be connected to V_A when the charge pump is on.
2. There is no I_A current consumption when the internal charge pump is enabled and only a decoupling capacitor is connected to the V_A pin.
3. All inputs at 0.4 or V_D – 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (Static I_{OUT} = 0 mA).
4. $\overline{\text{RGDT}}$ is not functional in this state.
5. The charge pump is recommended to be used only when V_D < 4.5 V. When the charge pump is not used, V_A should be applied to the device before V_D is applied on power up if driven from separate supplies.

Table 5. AC Characteristics

(V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, see Figure 16 on page 15)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate[1]	Fs	Fs = F_{PLL2}/5120	7.2	—	11.025	KHz
PLL1 Output Clock Frequency[1]	F_{PLL1}	F_{PLL1} = F_{MCLK} • M1/N1	36	—	58	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	0	—	Hz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[2]	V_{FS}		—	1	—	V_{PEAK}
Receive Full Scale Level[2,3]	V_{FS}		—	1	—	V_{PEAK}
Dynamic Range[4]	DR	ACT = 0, DCT = 10 (FCC) I_L = 100 mA	—	82	—	dB
Dynamic Range[4]	DR	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	83	—	dB
Dynamic Range[4]	DR	ACT = 1, DCT = 11(CTR21) I_L = 60 mA	—	84	—	dB
Transmit Total Harmonic Distortion[5]	THD	ACT = 0, DCT = 10 (FCC) I_L = 100 mA	—	–85	—	dB
Transmit Total Harmonic Distortion[5]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–76	—	dB
Receive Total Harmonic Distortion[5]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–74	—	dB
Receive Total Harmonic Distortion[5]	THD	ACT = 1, DCT = 11 (CTR21) I_L = 60 mA	—	–82	—	dB
Dynamic Range (call progress AOUT)	DR_{AO}	VIN = 1 kHz	60	—	—	dB
THD (call progress AOUT)	THD_{AO}	VIN = 1 kHz	—	1.0	—	%
AOUT Full Scale Level			—	0.75 V_D	—	V_{PP}
AOUT Output Impedance			—	10	—	kΩ
Mute Level (call progress AOUT)			–90	—	—	dBFS
Dynamic Range (caller ID mode)	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	60	—	dB
Caller ID Full Scale Level (0 dB gain)	V_{CID}		—	0.8	—	V_{PEAK}

Notes:

1. See Figure 23 on page 28.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. Receive full scale level will produce –0.9 dBFS at SDO.
4. DR = 20 • log |Vin| + 20 • log (RMS signal/RMS noise). Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. Vin = 1 KHz, –3 dBFS, Fs = 10300 Hz.
5. THD = 20 • log (RMS distortion/RMS signal). Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 6.0	V
Input Current, Si3021 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Switching Characteristics—General Inputs
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade, C_L = 20 pF)

Parameter[1]	Symbol	Min	Typ	Max	Unit
Cycle Time, MCLK	t_{mc}	16.67	—	1000	ns
MCLK Duty Cycle	t_{dty}	40	50	60	%
Rise Time, MCLK	t_r	—	—	5	ns
Fall Time, MCLK	t_f	—	—	5	ns
MCLK Before $\overline{\text{RESET}}$ ↑	t_{mr}	10	—	—	cycles
$\overline{\text{RESET}}$ Pulse Width[2]	t_{rl}	250	—	—	ns
M0, M1 Before $\overline{\text{RESET}}$↑[3]	t_{mxr}	20	—	—	ns

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width is the greater of 250 ns or 10 MCLK cycle times.
3. M0 and M1 are typically connected to V_D or GND and should not be changed during normal operation.

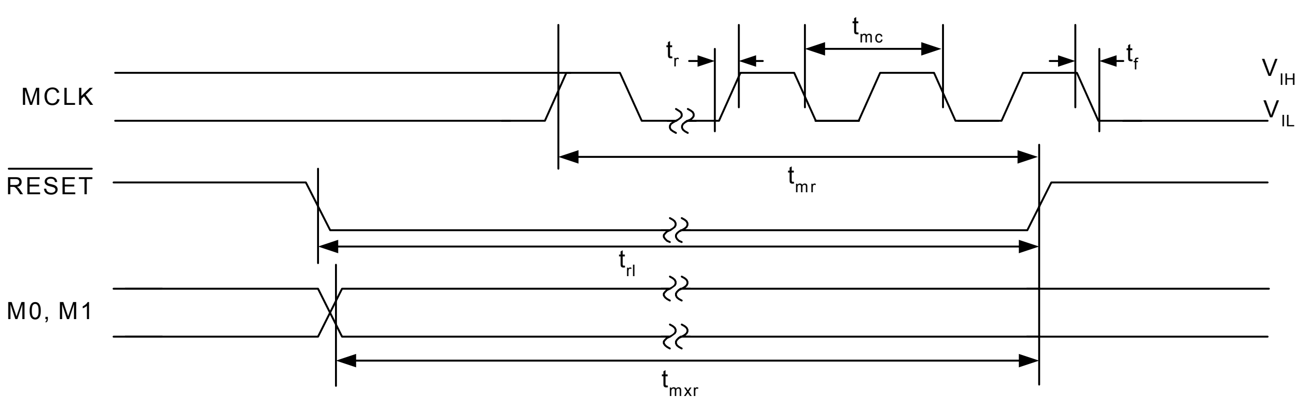


Figure 2. General Inputs Timing Diagram

Table 8. Switching Characteristics—Serial Interface (DCE = 0)
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK duty cycle	t_{dty}	—	50	—	%
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d1}	—	—	10	ns
Delay time, SCLK ↑ to SDO valid	t_{d2}	—	—	20	ns
Delay time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d3}	—	—	10	ns
Setup time, SDI before SCLK ↓	t_{su}	25	—	—	ns
Hold time, SDI after SCLK ↓	t_h	20	—	—	ns
Setup time, FC ↑ before SCLK ↑	t_{sfc}	40	—	—	ns
Hold time, FC ↑ after SCLK ↑	t_{hfc}	40	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.					

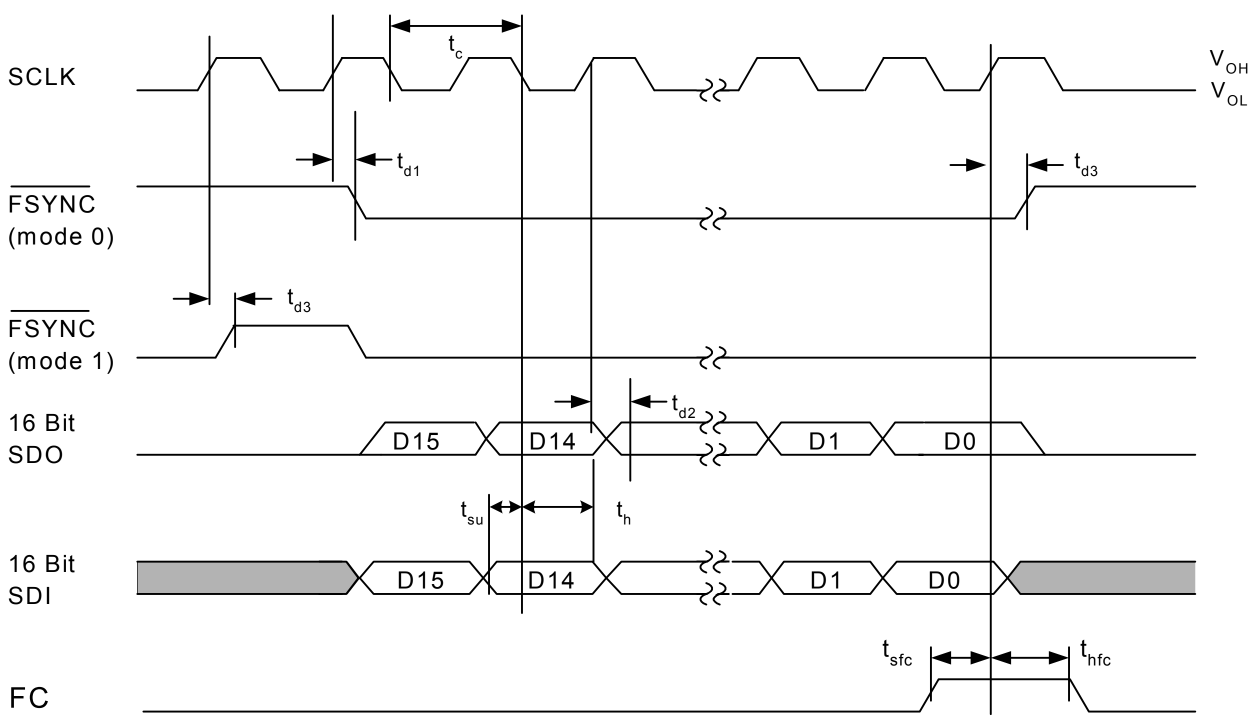


Figure 3. Serial Interface Timing Diagram (DCE = 0)

Table 9. Switching Characteristics—Serial Interface (DCE = 1, FSD = 0)
(V_A = Charge Pump, V_D = 3.0 to 5.25 V, T_A = 0 to 70°C for K-Grade, C_L = 20 pF)

Parameter[1,2]	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{FSYNC}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{FSYNC}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c – 20$	—	$0.25t_c + 20$	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{RGDT}$ ↓	t_{d5}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{RGDT}$ ↑	t_{d6}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D – 0.4$ V, V_{IL} = 0.4 V.
2. Refer to the section "Multiple Device Support," on page 30 for functional details.

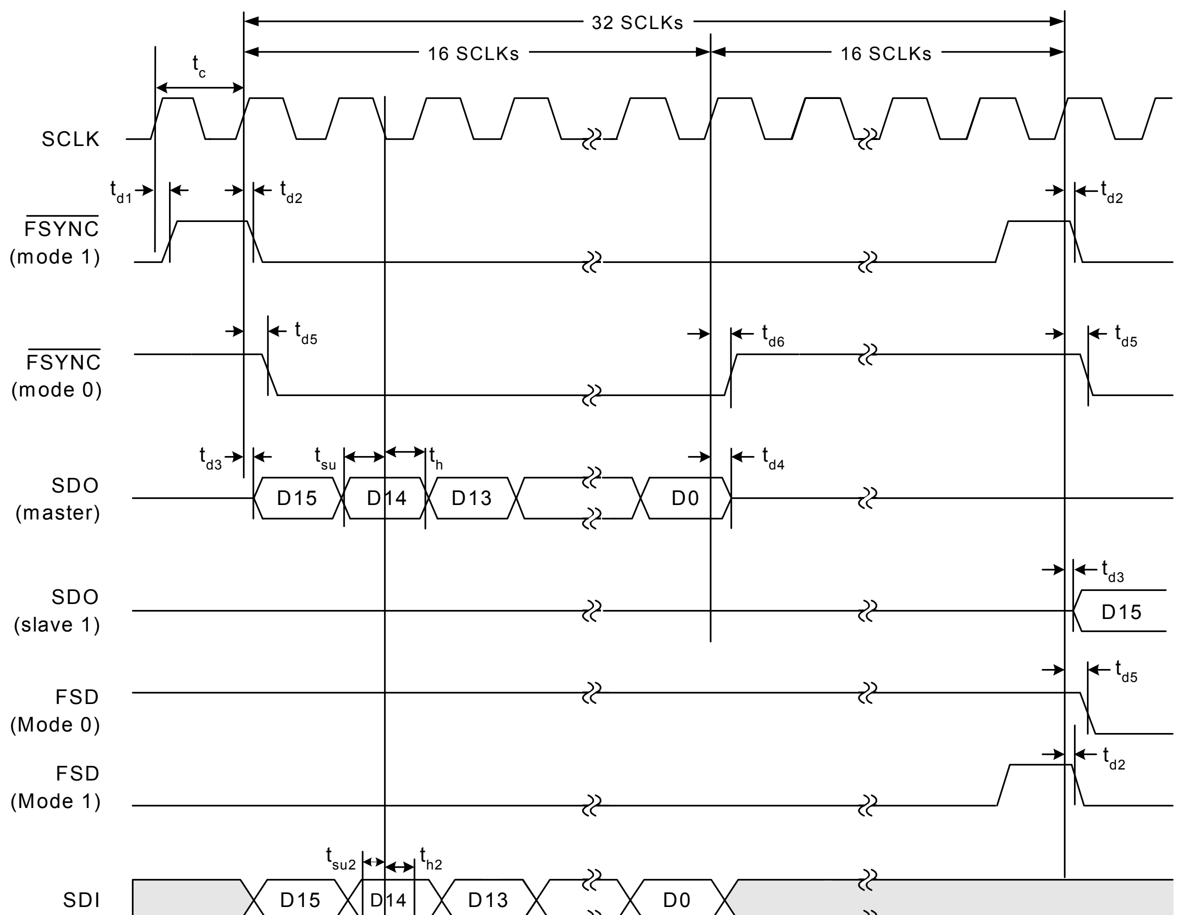


Figure 4. Serial Interface Timing Diagram (DCE = 1, FSD = 0)

Table 10. Switching Characteristics—Serial Interface (DCE = 1, FSD = 1)
(V_D = 3.0 to 5.25 V, T_A = 70°C for K-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Cycle Time, SCLK	t_c	354	1/256 Fs	—	ns
SCLK Duty Cycle	t_{dty}	—	50	—	%
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↑	t_{d1}	—	—	10	ns
Delay Time, SCLK ↑ to $\overline{\text{FSYNC}}$ ↓	t_{d2}	—	—	10	ns
Delay Time, SCLK ↑ to SDO valid	t_{d3}	$0.25t_c - 20$	—	$0.25t_c + 20$	ns
Delay Time, SCLK ↑ to SDO Hi-Z	t_{d4}	—	—	20	ns
Delay Time, SCLK ↑ to $\overline{\text{RGDT}}$ ↓	t_{d5}	—	—	20	ns
Setup Time, SDO Before SCLK ↓	t_{su}	25	—	—	ns
Hold Time, SDO After SCLK ↓	t_h	20	—	—	ns
Setup Time, SDI Before SCLK	t_{su2}	25	—	—	ns
Hold Time, SDI After SCLK	t_{h2}	20	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D - 0.4$ V, V_{IL} = 0.4 V.
2. Refer to "Multiple Device Support," on page 30 for functional details.

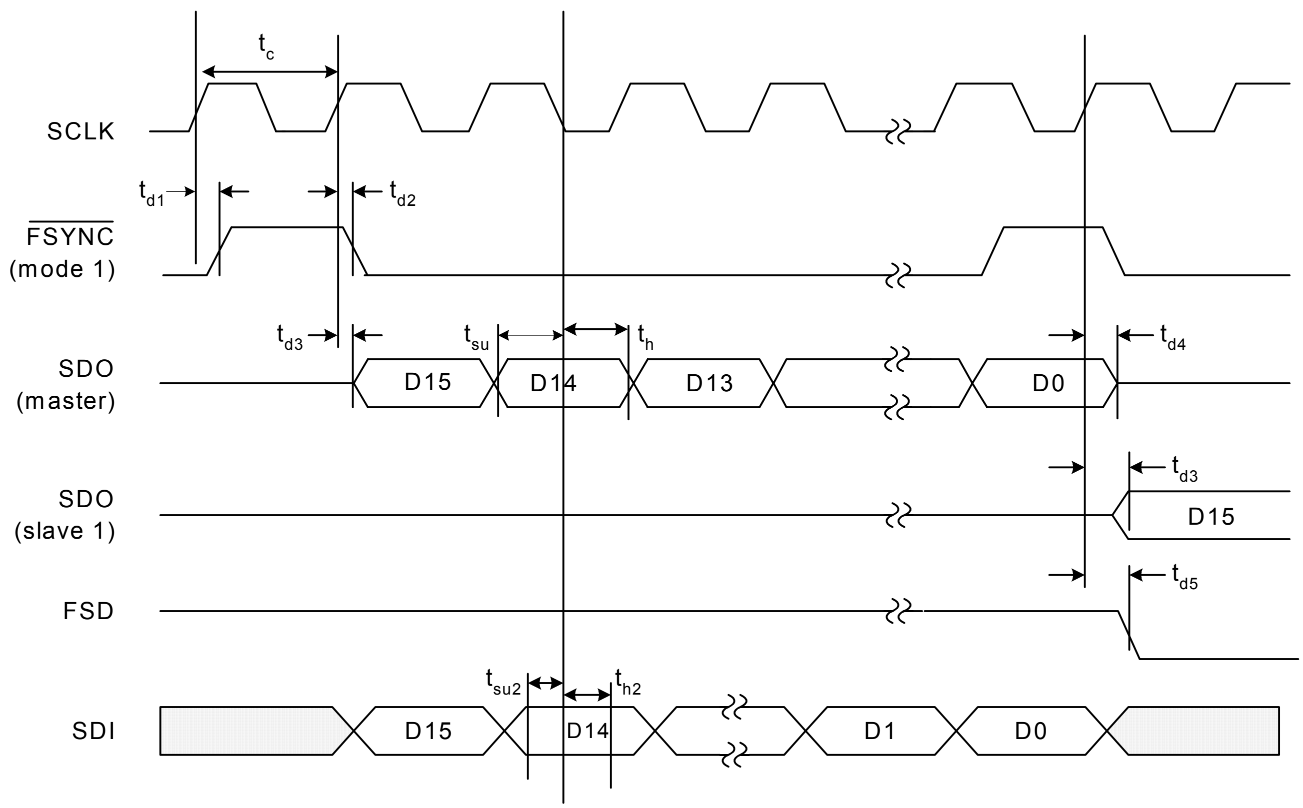


Figure 5. Serial Interface Timing Diagram (DCE = 1, FSD = 1)

Table 11. Digital FIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 5.25 V, Sample Rate = 8 kHz, T_A = 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	sec
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 6, 7, 8, and 9.					

Table 12. Digital IIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 5.25 V, Sample Rate = 8 kHz, T_A = 70°C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	sec
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 10, 11, 12, and 13. Figures 14 and 15 show group delay versus input frequency.					

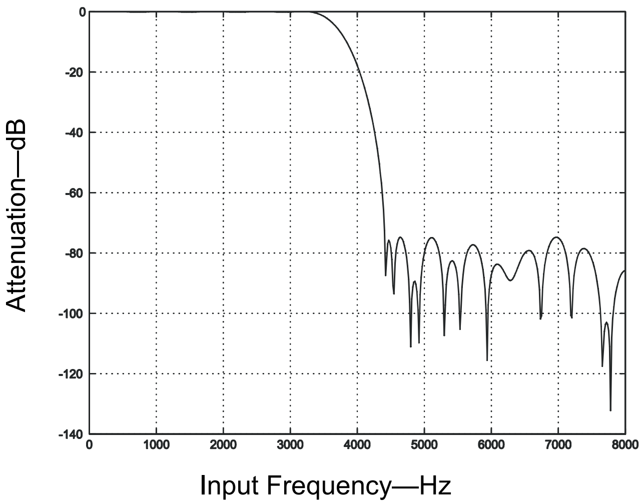


Figure 6. FIR Receive Filter Response

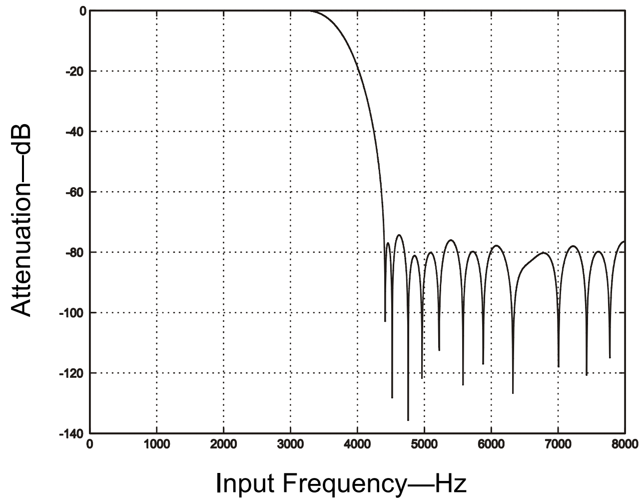


Figure 8. FIR Transmit Filter Response

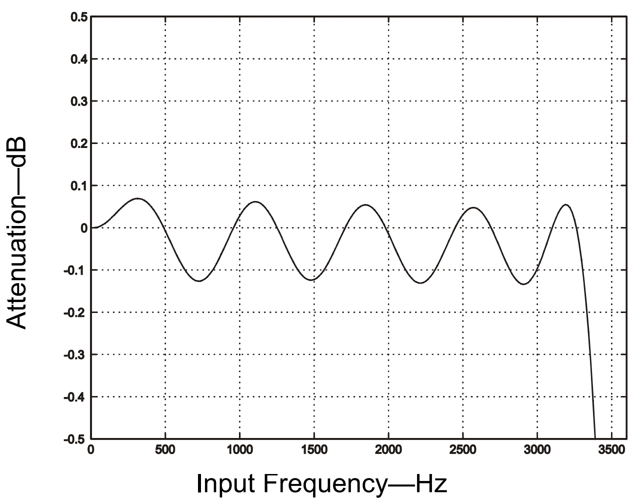


Figure 7. FIR Receive Filter Passband Ripple

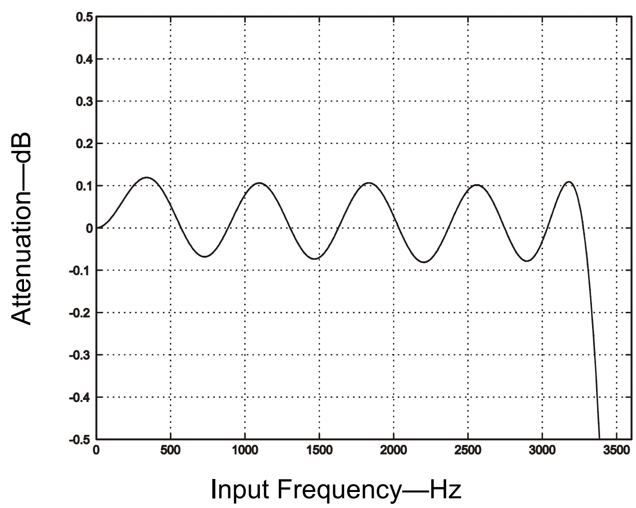


Figure 9. FIR Transmit Filter Passband Ripple

For Figures 6–9, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(0.1\ dB)}$ = 0.4125 Fs

$F_{(-3\ dB)}$ = 0.45 Fs

where Fs is the sample frequency.

For Figures 10–13, all filter plots apply to a sample rate of Fs = 8 kHz. The filters scale with the sample rate as follows:

$F_{(-3\ dB)}$ = 0.45 Fs

where Fs is the sample frequency.

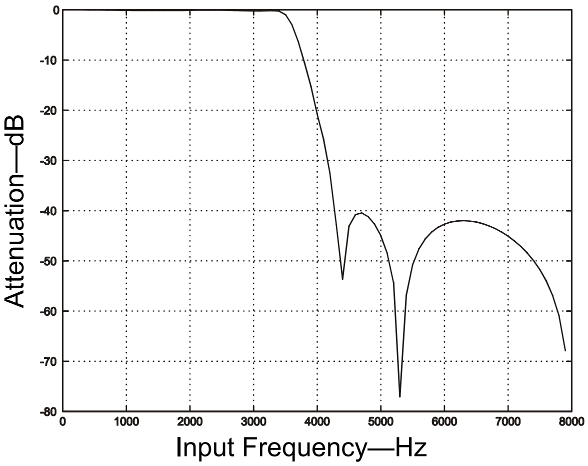


Figure 10. IIR Receive Filter Response

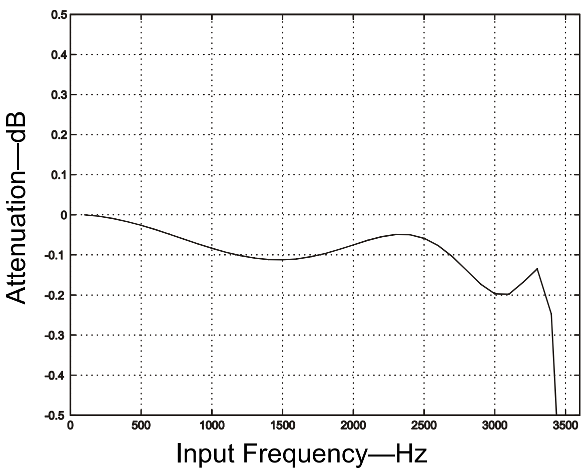


Figure 11. IIR Receive Filter Passband Ripple

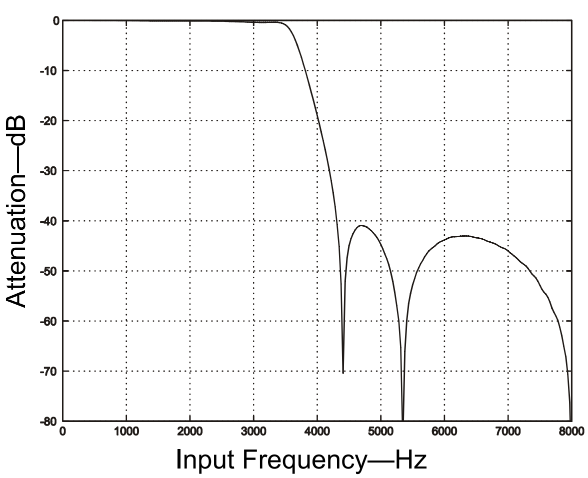


Figure 12. IIR Transmit Filter Response

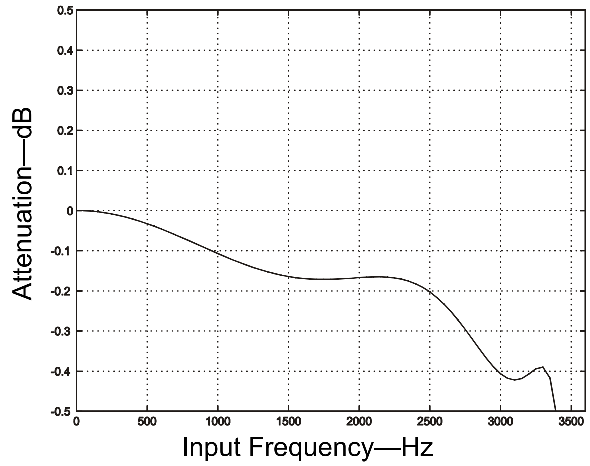


Figure 13. IIR Transmit Filter Passband Ripple

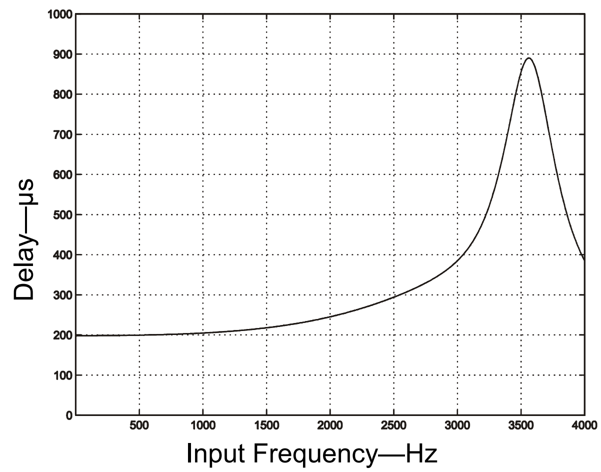


Figure 14. IIR Receive Group Delay

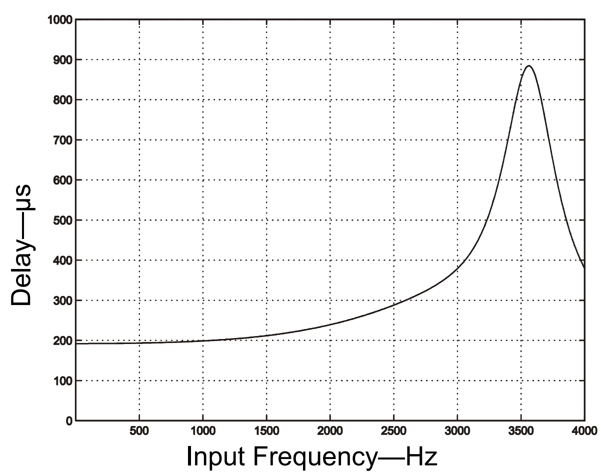
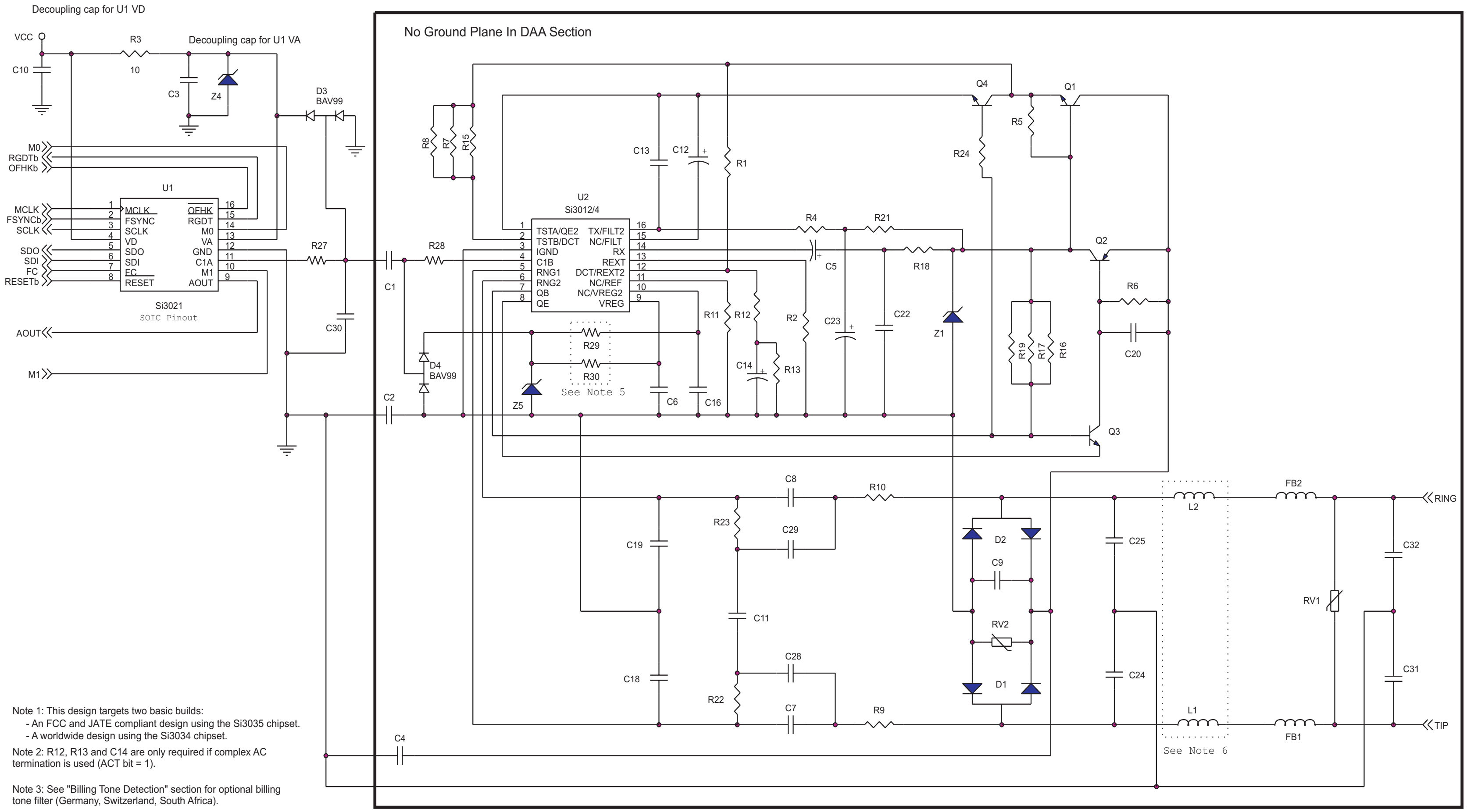


Figure 15. IIR Transmit Group Delay



Note 1: This design targets two basic builds:
- An FCC and JATE compliant design using the Si3035 chipset.
- A worldwide design using the Si3034 chipset.

Note 2: R12, R13 and C14 are only required if complex AC termination is used (ACT bit = 1).

Note 3: See "Billing Tone Detection" section for optional billing tone filter (Germany, Switzerland, South Africa).

Note 4: See Appendix for applications requiring UL 1950 3rd edition compliance.

Note 5: For Si3035 designs R29 is populated with a 0 ohm resistor and R30 is not installed. For Si3034 designs R29 is not installed and R30 is populated with a 0 ohm resistor.

Note 6: Please refer to Appendix B for information regarding L1 and L2.

Figure 16. Typical Application Circuit for the Dual Design Si3034 and Si3035

Bill of Materials

Table 13. Global Component Values

Component[1]	Value	Supplier(s)
C1,C4[2]	150 pF, 3 kV, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C2,C11,C23,C28,C29,C31,C32	Not Installed	
C3	0.22 µF, 16 V, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C5	0.1 µF, 50 V, X7R/Elec/Tant, ±20%	
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	
C7,C8	560 pF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic
C9	10 nF, 250 V, X7R, ±20%	
C12	0.22 µF, 16 V, Tant, ±20%	Panasonic
C13	0.47 µF, 16 V, X7R, ±20%	
C14	0.68 µF, 16 V, X7R/Elec/Tant, ±20%	
C18,C19	3.9 nF, 16 V, X7R, ±20%	
C20	0.01 µF, 16 V, X7R, ±20%	
C22	1800 pF, 50 V, X7R, ±20%	
C24,C25[2]	1000 pF, 3 kV, X7R, ±10%	
C30[3]	Not Installed	
D1,D2[4]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4	BAV99 Dual Diode, 70 V, 350 mW	Diodes, Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead	Murata
L1,L2[5]	330 µH, DCR <3 Ω, 120 mA, ±10%	Taiyo Yuden, ACT, Transtek Magnetics, Cooper Electronics
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild
Q4[6]	BCP56T1, NPN, 60 V, 1/2 W	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2[7]	Not Installed	
R1,R4,R21,R22,R23	Not Installed	
R2	402 Ω, 1/16 W, ±1%	
R3[8]	Not Installed	
R5	36 kΩ, 1/16 W, ±5%	
R6	120 kΩ, 1/16 W, ±5%	
R7,R8,R15,R16,R17,R19[9]	4.87 kΩ, 1/4 W, ±1%	
R9,R10	56 kΩ, 1/10 W, ±5%	
R11	10 kΩ, 1/16 W, ±1%	
R12	78.7 Ω, 1/16 W, ±1%	
R13	215 Ω, 1/16 W, ±1%	
R18	2.2 kΩ, 1/10 W, ±5%	
R24	150 Ω, 1/16 W, ±5%	
R27,R28	10 Ω, 1/10 W, ±5%	
R29	Not Installed	
R30	0 Ω, 1/10 W	
U1	Si3021	Silicon Labs
U2	Si3014	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	Vishay, OnSemiconductor, Rohm
Z4,Z5	Zener Diode, 5.6 V, 1/2 W	Diodes, Inc., OnSemiconductor, Fairchild

Notes:
1. The following reference designators were intentionally omitted: C15, C17, C21, C26, C27, R14, and R20.
2. Y2 class capacitors are needed for the Nordic requirements of EN60950 and may also be used to achieve surge performance of 5 kV or better.
3. Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
4. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.)
5. See Appendix B for additional considerations.
6. Q4 may require copper on board to meet 1/2 power requirement. (Contact transistor manufacturer for details.)
7. RV2 can be installed to improve performance from 2500 V to 3500 V for multiple longitudinal surges (270 V, MOV).
8. If the charge pump is not enabled (with the CPE bit in Register 6), VA must be 4.75 to 5.25 V. R3 can be installed with a 10 Ω, 1/10 W, ±5% if V_D is also 4.75 to 5.25 V.
9. The R7, R8, R15 and R16, R17, R19 resistors may each be replaced with a single resistor of 1.62 kΩ, 3/4 W, ±1%.

SILICON LABORATORIES

Table 14. FCC Component Values—Si3035 Chipset

Component[1]	Value	Supplier(s)
C1,C4[2]	150 pF, 3 kV, X7R,±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C2	Not Installed	
C3	0.22 µF, 16 V, X7R, ±20%	
C5	1.0 µF, 16 V, Elec/Tant, ±20%	
C6,C10,C16	0.1 µF, 16 V, X7R, ±20%	
C9,C28,C29	15 nF, 250 V, X7R, ±20%	Novacap, Johanson, Murata, Panasonic
C11	39 nF, 16 V, X7R, ±20%	
C7,C8,C12,C13,C14 C18,C19,C20,C22,C23[3]	Not Installed	
C24,C25,C31,C32[2,4]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic
C30[5]	Not Installed	
D1,D2[6]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4	BAV99 Dual Diode, 70 V, 350 mW	Diodes, Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead	Murata
L1,L2	0 Ω, 1/10 W	
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild
Q4	Not Installed	
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI
RV2	240 V, MOV	Panasonic
R1	51 Ω, 1/2 W, ±5%	
R2	15 Ω, 1/4 W, ±5%	
R3[7]	Not Installed	
R4,R18,R21	301 Ω, 1/10 W, ±1%	
R5,R6	36 kΩ, 1/10 W, ±5%	
R7,R8,R11[3],R12,R13,R15 R16,R17,R19,R24	Not Installed	
R9,R10	2 kΩ, 1/10 W, ±5%	
R22,R23	20 kΩ, 1/10 W, ±5%	
R27,R28	10 Ω, 1/10 W, ±5%	
R29	0 Ω, 1/10 W	
R30	Not Installed	
U1	Si3021	Silicon Labs
U2	Si3012	Silicon Labs
Z1	Zener Diode, 18 V	Vishay, OnSemiconductor, Rohm
Z4,Z5	Zener Diode, 5.6 V, 1/2 W	Diodes, Inc., OnSemiconductor, Fairchild

Notes:

1. The following reference designators were intentionally omitted: C15, C17, C21, C26, C27, R14, and R20.
2. Y2 class capacitors may also be used to achieve surge performance of 5 kV or better.
3. If JATE support is required using the Si3035 chipset, C23 should be populated with a 0.1 µF, 16 V, Tant/Elec/X7R, ±20% and R11 should be populated with a 2.7 nF, 16 V, X7R, ±20% capacitor.
4. Alternate population option is C24, C25 (2200 pF, 3 kV, X7R, ±10% and C31, C32 not installed).
5. Install only if needed for improved radiated emissions performance (10 pF, 16 V, NPO, ±10%).
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.).
7. If the charge pump is not enabled (with the CPE bit in Register 6), V_A must be 4.75 to 5.25 V. R3 can be installed with a 10 Ω, 1/10 W, ±5% if V_D is also 4.75 to 5.25 V.

Analog Output

Figure 17 illustrates an optional application circuit to support the analog output capability of the Si3034 for call progress monitoring purposes. The ARM bits in Register 6 allow the receive path to be attenuated by 0 dB, –6 dB, or –12 dB. The ATM bits, which are also in Register 6, allow the transmit path to be attenuated by –20 dB, –26 dB, or –32 dB. Both the transmit and receive paths can also be independently muted.

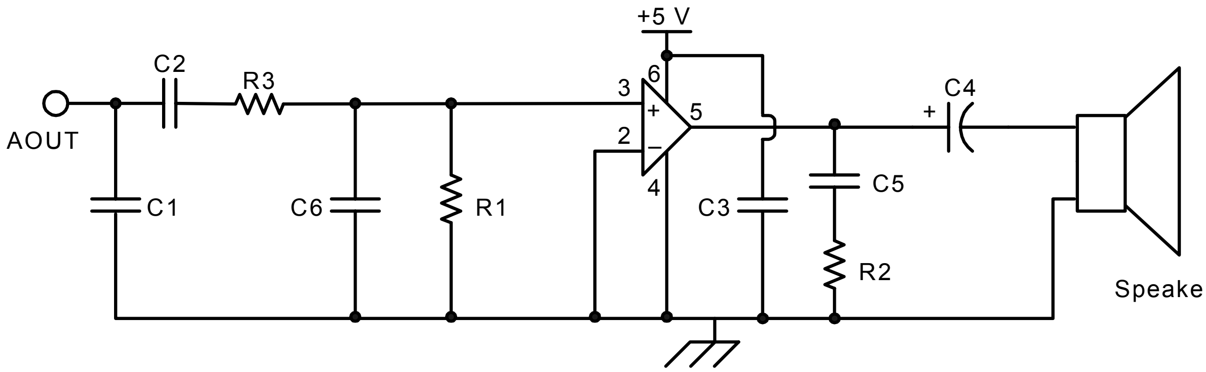


Figure 17. Optional Connection to AOUT for a Call Progress Speaker

Table 15. Component Values—Optional Connection to AOUT

Symbol	Value
C1	2200 pF, 16 V, ±20%
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

Functional Description

The Si3034 is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The device implements Silicon Laboratories' proprietary ISOcap technology which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two 16-pin small outline packages (SOIC or TSSOP).

The Si3034 chipset can be fully programmed to meet international requirements and is compliant with FCC, CTR21, JATE, and various other country-specific PTT specifications as shown in Table 16. In addition, the Si3034 has been designed to meet the most stringent worldwide requirements for out-of-band energy, emissions, immunity, lightning surges, and safety. Typical Si3034 designs implement a dual layout (see Figure 16) capable of two population options:

- FCC Compliant Population—This population option removes the external devices needed to support non-FCC countries. The FCC/JATE DAA Si3035 chipset is used.
- Globally Compliant Population—This population option targets global DAA requirements. This Si3034 international DAA chipset is populated, and the external devices required for the FCC-only population option are removed.

Table 16. Country Specific Register Settings

Register	16					17	18
Country	**OHS**	**ACT**	**DCT[1:0]**	**RZ**	**RT**	**LIM[1:0]**	**VOL[1:0]**
Argentina	0	0	10	0	0	00	00
Australia[1]	1	1	01	0	0	00	00
Austria	0	0 or 1	11	0	0	11	00
Bahrain	0	0	10	0	0	00	00
Belgium	0	0 or 1	11	0	0	11	00
Brazil[1]	0	0	01	0	0	00	00
Bulgaria	0	1	11	0	0	11	00
Canada	0	0	10	0	0	00	00
Chile	0	0	10	0	0	00	00
China[1]	0	0	01	0	0	00	00
Colombia	0	0	10	0	0	00	00
Croatia	0	1	11	0	0	11	00
CTR21[1,2]	0	0 or 1	11	0	0	11	00
Cyprus	0	1	11	0	0	11	00
Czech Republic	0	1	11	0	0	11	00
Denmark	0	0 or 1	11	0	0	11	00
Ecuador	0	0	10	0	0	00	00
Egypt[1]	0	0	01	0	0	00	00
El Salvador	0	0	10	0	0	00	00
Finland	0	0 or 1	11	0	0	11	00
France	0	0 or 1	11	0	0	11	00
Germany	0	0 or 1	11	0	0	11	00
Greece	0	0 or 1	11	0	0	11	00

Note:

1. See "DC Termination Considerations," on page 23 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current ≥ 20 mA.

Table 16. Country Specific Register Settings (Continued)

Register	16					17	18
Country	**OHS**	**ACT**	**DCT[1:0]**	**RZ**	**RT**	**LIM[1:0]**	**VOL[1:0]**
Guam	0	0	10	0	0	00	00
Hong Kong	0	0	10	0	0	00	00
Hungary	0	0	10	0	0	00	00
Iceland	0	0 or 1	11	0	0	11	00
India	0	0	10	0	0	00	00
Indonesia	0	0	10	0	0	00	00
Ireland	0	0 or 1	11	0	0	11	00
Israel	0	0 or 1	11	0	0	11	00
Italy	0	0 or 1	11	0	0	11	00
Japan[1]	0	0	01	0	0	00	00
Jordan[1]	0	0	01	0	0	00	00
Kazakhstan[1]	0	0	01	0	0	00	00
Kuwait	0	0	10	0	0	00	00
Latvia	0	0 or 1	11	0	0	11	00
Lebanon	0	0 or 1	11	0	0	11	00
Luxembourg	0	0 or 1	11	0	0	11	00
Macao	0	0	10	0	0	00	00
Malaysia[1,3]	0	0	01	0	0	00	00
Malta	0	0 or 1	11	0	0	11	00
Mexico	0	0	10	0	0	00	00
Morocco	0	0 or 1	11	0	0	11	00
Netherlands	0	0 or 1	11	0	0	11	00
New Zealand	0	1	10	0	0	00	00
Nigeria	0	0 or 1	11	0	0	11	00
Norway	0	0 or 1	11	0	0	11	00
Oman[1]	0	0	01	0	0	00	00
Pakistan[1]	0	0	01	0	0	00	00
Peru	0	0	10	0	0	00	00
Philippines[1]	0	0	01	0	0	00	00
Poland	0	0	10	1	1	00	00
Portugal	0	0 or 1	11	0	0	11	00
Romania	0	0	10	0	0	00	00
Russia[1]	0	0	01	0	0	00	00
Saudi Arabia	0	0	10	0	0	00	00
Singapore	0	0	10	0	0	00	00
Slovakia	0	0	10	0	0	00	00

Note:

1. See "DC Termination Considerations," on page 23 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current ≥ 20 mA.

Table 16. Country Specific Register Settings (Continued)

Register	16					17	18
Country	**OHS**	**ACT**	**DCT[1:0]**	**RZ**	**RT**	**LIM[1:0]**	**VOL[1:0]**
Slovenia	0	0	10	1	1	00	00
South Africa	1	0	10	1	0	00	00
South Korea	0	0	10	0	0	00	00
Spain	0	0 or 1	11	0	0	11	00
Sweden	0	0 or 1	11	0	0	11	00
Switzerland	0	0 or 1	11	0	0	11	00
Syria[1]	0	0	01	0	0	00	00
Taiwan[1]	0	0	01	0	0	00	00
Thailand[1]	0	0	01	0	0	00	00
UAE	0	0	10	0	0	00	00
United Kingdom	0	0 or 1	11	0	0	11	00
USA	0	0	10	0	0	00	00
Yemen	0	0	10	0	0	00	00

Note:
1. See "DC Termination Considerations," on page 23 for more information.
2. CTR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
3. Supported for loop current ≥ 20 mA.

Initialization

When the Si3034 is initially powered up, the $\overline{\text{RESET}}$ pin should be asserted. When the $\overline{\text{RESET}}$ pin is deasserted, the registers will have default values. This reset condition guarantees the line-side chip (Si3014) is powered down with no possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined below:

1. Program the PLLs with registers 7 to 9 (N1[7:0], M1[7:0], N2[3:0], and M2[3:0]) to the appropriate divider ratios for the supplied MCLK frequency and desired sample rate, as defined in "Clock Generation Subsystem," on page 27.
2. Wait until the PLLs are locked. This time is between 100 µS and 1 ms.
3. Write an 80H into Register 6. This enables the charge pump for the V_A pin, powers up the line-side chip (Si3014), and enables the AOUT for call progress monitoring.
4. Set the desired line interface parameters (i.e., DCT[1:0], ACT, OHS, RT, LIM[1:0], and VOL[1:0]) as defined by "Country Specific Register Settings" shown in Table 16.

After this procedure is complete, the Si3034 is ready for ring detection and off-hook.

On-Chip Charge Pump

The Si3034 has an on-chip charge pump that can produce the V_A supply needed by the ISOcap communication link. This on-chip power supply can be enabled by setting bit 7 in Register 6 to 1.

Before enabling the line-side chip, care should be taken to ensure it is properly powered. If the on-chip charge pump is used to provide the V_A supply, R3 should not be populated. If the on-chip charge pump is not used, the V_A supply may be powered from the digital power supply (V_D). In this case, V_D should be at least 4.75 V, and R3 should be populated. A separate 5 V power supply may also be used for the V_A supply, in which case R3 should not be populated.

Isolation Barrier

The Si3034 achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' proprietary ISOcap signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in Figure 16 on page 15, the C1, C4, C24, and C25 capacitors isolate the Si3021 (DSP-side) from the Si3014 (line-side). All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier. Y2 class capacitors may be used for the isolation barrier to achieve surge performance of 5 kV or greater.

The ISOcap communications link is disabled by default. To enable it, the PDL bit in Register 6 must be cleared.

No communication between the Si3021 and Si3014 can occur until this bit is cleared. The clock generator **must** be programmed to an acceptable sample rate prior to clearing the PDL bit.

Off-Hook

The communication system generates an off-hook command by applying logic 0 to the $\overline{\text{OFHK}}$ pin or by setting the OH bit in Register 5. The $\overline{\text{OFHK}}$ pin must be enabled by setting the OHE bit in Register 5. With $\overline{\text{OFHK}}$ at logic 0, the system is in an off-hook state.

The off-hook state is used to seize the line for incoming/outgoing calls and can also be used for pulse dialing. With $\overline{\text{OFHK}}$ at logic 1, negligible dc current flows through the hookswitch. When a logic 0 is applied to the $\overline{\text{OFHK}}$ pin, the hookswitch transistor pair, Q1 & Q2, turn on. This applies a termination impedance across TIP and RING and causes dc loop current to flow. The termination impedance has both an ac and dc component.

When executing an off-hook sequence, the Si3034 requires 1548/Fs seconds to complete the off-hook and provide phone-line data on the serial link. This includes the 12/Fs filter group delay. If necessary, for the shortest delay, a higher Fs may be established prior to executing the off-hook, such as an Fs of 10.286 kHz. The delay allows for line transients to settle prior to normal use.

DC Termination

The Si3034 has three programmable dc termination modes which are selected with the DCT[1:0] bits in Register 16.

Japan Mode (DCT[1:0] = 01 b), shown in Figure 18, is a lower voltage mode and supports a transmit full scale level of –2.71 dBm. Higher transmit levels for DTMF dialing are also supported. See "DTMF Dialing," on page 24. The low voltage requirement is dictated by countries such as Japan and Malaysia.

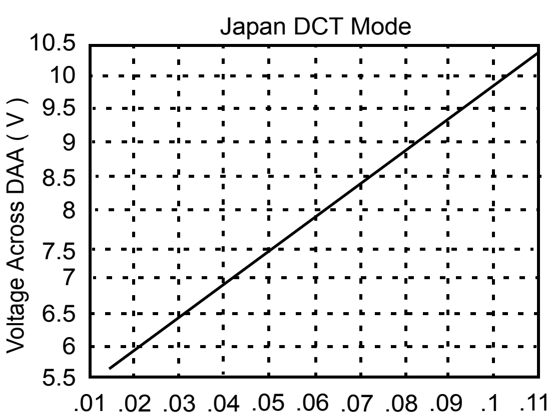


Figure 18. Japan Mode I/V Characteristics

FCC Mode (DCT[1:0] = 10 b), shown in Figure 19, is the default dc termination mode and supports a transmit full scale level of –1 dBm at TIP and RING. This mode meets FCC requirements in addition to the requirements of many other countries.

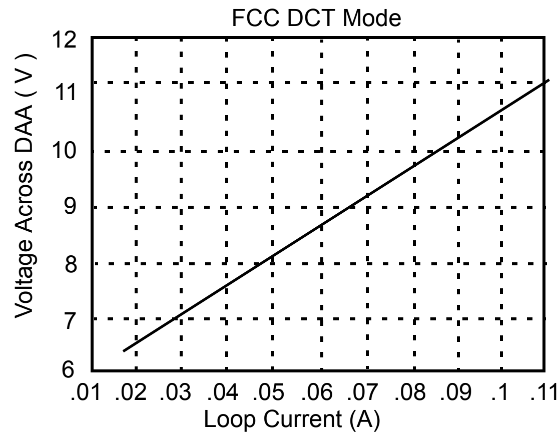


Figure 19. FCC Mode I/V Characteristics

CTR21 Mode (DCT[1:0] = 11 b), shown in Figure 20, provides current limiting, while maintaining a transmit full scale level of –1 dBm at TIP and RING. In this mode, the dc termination will current limit before reaching 60 mA.

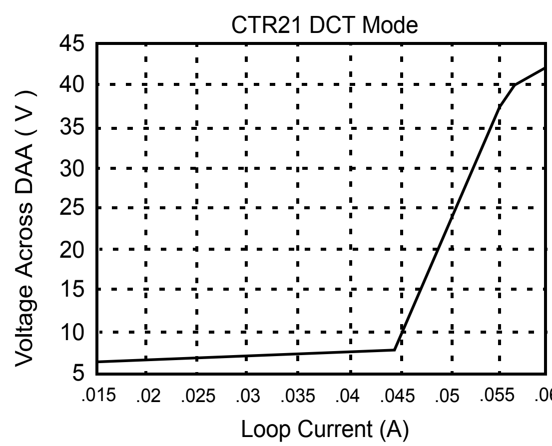


Figure 20. CTR21 Mode I/V Characteristics

AC Termination

The Si3034 has two ac termination impedances which are selected with the ACT bit in Register 16.

ACT = 0 is a real, nominal 600 Ω termination which satisfies the impedance requirements of FCC part 68, JATE, and other countries. This real impedance is set by circuitry internal to the Si3034 as well as the resistor

R2 connected to the REXT pin.

ACT = 1 is a complex impedance which satisfies the impedance requirements of Australia, New Zealand, South Africa, CTR21, and some European NET4 countries such as the UK and Germany. This complex impedance is set by circuitry internal to the Si3034 as well as the complex network formed by R12, R13, and C14 connected to the REXT2 pin.

DC Termination Considerations

Under certain line conditions, it may be beneficial to use other dc termination modes not intended for a particular world region. For instance, in countries that comply with the CTR21 standard, improved distortion characteristics can be seen for very low loop current lines by switching to FCC mode. Thus, after going off-hook in CTR21 mode, the loop current monitor bits (LCS[3:0]) may be used to measure the loop current, and if LCS[3:0] < 3, it is recommended that FCC mode be used.

Additionally, for very low voltage countries, such as Japan and Malaysia, the following procedure may be used to optimize distortion characteristics and maximize transmit levels:

1. When first going off-hook, use the Japan mode with the VOL bits (Register 18, bits 4:3) set to 01.
2. Measure the loop current using the LCS[3:0] bits.
3. If LCS[3:0]] ≤ 2, maintain the current settings and proceed with normal operation.
4. If LCS[3:0] ≥ 3, switch to FCC mode, set the VOL bit to 0, and proceed with normal operation.

Note: A single decision of dc termination mode following off-hook is appropriate for most applications. However, during PTT testing, a false dc termination I/V curve may be generated if the dc I/V curve is determined following a single off-hook event.

Finally, Australia has separate dc termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This will satisfy the Australian dc termination requirements.

Ring Detection

The ring signal is capacitively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3034 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal. See “Caller ID” on page 26. The ring detection threshold is programmable with the RT bit in Register 16.

The ring detector output can be monitored in one of three ways. The first method uses the $\overline{\text{RGDT}}$ pin. The second method uses the register bits RDTP, RDTN, and RDT in Register 5. The final method uses the SDO output.

The DSP must detect the frequency of the ring signal in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

The ring detector mode is controlled by the RFWE bit of Register 18. When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ringing signals are detected. A positive ringing signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. RNG1 and RNG2 are pins 5 and 6 of the Si3014. Conversely, a negative ringing signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

When the RFWE bit is 0, the $\overline{\text{RGDT}}$ pin will toggle active low when the ring signal is positive. When the RFWE bit is 1, the $\overline{\text{RGDT}}$ pin will toggle active low when the ring signal is positive or negative. This makes the ring signal appear to be twice the frequency of the ringing waveform.

The second method uses the ring detect bits (RDTP, RDTW, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. Whenever the signal RNG1-RNG2 is above the positive ring threshold the RDTP bit is set. Whenever the signal RNG1-RNG2 is below the negative ring threshold the RDTN bit is set. When the signal RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is a 0 or a 1, a positive ringing signal will set the RDT bit for a period of time. The RDT bit will not be set for a negative ringing signal.

The RDT bit acts as a one shot. Whenever a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter counting down to zero, then the RDT bit will return to zero. The length of this count (in seconds) is 65536 divided by the sample rate. The RDT will also be reset to zero by an off-hook event.

The third method uses the serial communication interface to transmit ring data. If the ISOCap is active (PDL=0) and the device is not off-hook or not in on-hook line monitor mode, the ring data will be presented on SDO. The waveform on SDO depends on the state of the RFWE bit.

When the RFWE bit is 0, SDO will be –32768 (0x8000) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, SDO will transition to +32767 while the ring signal is positive, then go back to –32768 while the ring is near zero and negative. Thus a near square wave is presented on SDO that swings from –32768 to +32767 in cadence with the ring signal.

When the RFWE bit is 1, SDO will sit at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring goes positive, SDO will transition to +32767. When the ring signal goes near zero, SDO will remain near 1228. Then as the ring goes negative, the SDO will transition to –32768. This will repeat in cadence with the ring signal.

The best way to observe the ring signal on SDO is simply to observe the MSB of the data. The MSB will toggle in cadence with the ring signal independent of the ring detector mode. This is adequate information for determining the ring frequency. The MSB of SDO will toggle at the same frequency as the ring signal.

Ringer Impedance

The ring detector in many DAAs is ac coupled to the line with a large, 1 µF, 250 V decoupling capacitor. The ring detector on the Si3034 is also capacitively coupled to the line, but it is designed to use smaller, less expensive capacitors (C7, C8). Inherently, this network produces a high ringer impedance to the line of approximately 800 to 900 kΩ. This value meets the majority of country PTT specifications, including FCC and CTR21.

Several countries including Poland, South Africa, and Slovenia, require a maximum ringer impedance that can be met with an internally synthesized impedance by setting the RZ bit in Register 16.

DTMF Dialing

In CTR21 dc termination mode, the DIAL bit in Register 18 should be set during DTMF dialing if the LCS[3:0] bits are less than 6. Setting this bit increases headroom for large signals. This bit should not be used during normal operation nor if the LCS[3:0] bits are greater than 5.

In Japan dc termination mode, the Si3021 device attenuates the transmit output by 1.7 dB to meet headroom requirements. This attenuation can be removed when DTMF dialing is desired in this mode. When in the FCC dc termination mode, the FJM bit in Register 18 will enable the Japan dc termination mode without the 1.7 dB attenuation. Increased distortion may be observed, which is acceptable during DTMF dialing. After DTMF dialing is complete, the attenuation should be enabled by setting the Japan dc termination mode DCT[1:0] = 01b. The FJM bit has no effect in Japan dc termination mode.

Higher DTMF levels may also be achieved if the amplitude is increased and the peaks of the DTMF signal are clipped at digital full scale (as opposed to wrapping). Clipping the signal will produce some distortion and intermodulation of the signal. Generally, somewhat increased distortion (between 10–20%) is acceptable during DTMF signaling. Several dB higher DTMF levels can be achieved with this technique, compared with a digital full scale peak signal.

Pulse Dialing

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity, including make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are a number of issues in meeting these requirements.

The Si3034 dc holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed, resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional way of dealing with this problem is to put a parallel RC shunt across the hookswitch relay. The capacitor is large (~1 µF, 250 V) and relatively expensive. In the Si3034, the OHS bit in Register 16 can be used to slowly ramp down the loop current to pass these tests without requiring additional components.

Billing Tone Detection

"Billing tones" or "Metering Pulses" generated by the central office can cause modem connection difficulties. The billing tone is typically either a 12 KHz or 16 KHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors related to the modem data. The Si3034 chipset has a feature which allows the device to provide feedback as to whether a billing tone has occurred and when it ends.

Billing tone detection is enabled by setting the BTE bit (Register 17, bit 2). Billing tones less than 1.1 V_{PK} on the line will be filtered out by the low pass digital filter on the Si3034. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device (Si3014). When the BTD bit is set, the dc termination is changed to an 800 Ω dc impedance. This ensures minimum line voltage levels even in the presence of billing tones.

The OVL bit (Register 19) should be monitored (polled) following a billing tone detection. When the OVL bit returns to 0, indicating that the billing tone has passed, the BTE bit should be written to 0 to return the dc termination to its original state. It will take approximately one second to return to normal dc operating conditions. The BTD and ROV bits are sticky, and they must be written to 0 to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to reenable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA will remain off-hook during a billing tone event, the received data from the line will be corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/customers.

Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

Billing Tone Filter (Optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The Si3034 can remain off-hook during a billing tone event, but modem data will be lost in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 KHz and one at 16 KHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 21 shows an example of a billing tone filter.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 KHz and 16 KHz.

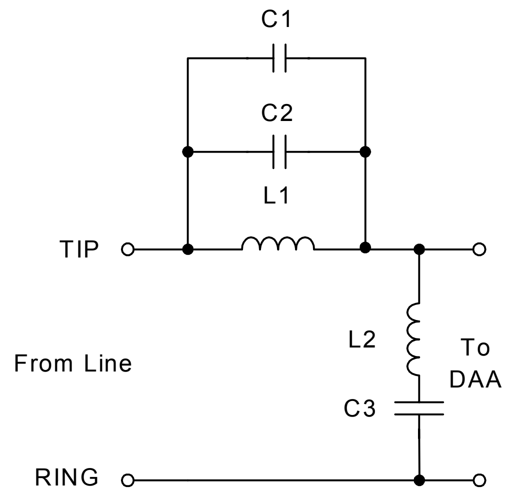


Figure 21. Billing Tone Filter

Table 17. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 µF, 50 V, ±10%
C3	0.01 µF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

The billing tone filter effects the ac termination and return loss. The current complex ac termination will pass worldwide return loss specifications both with and without the billing tone filter by at least 3 dB. The ac termination is optimized for frequency response and hybrid cancellation, while having greater than 4 dB of margin with or without the dongle for South Africa, Australia, CTR21, German, and Swiss country-specific specifications.

On-Hook Line Monitor

The Si3034 allows the user to receive line activity when in an on-hook state. The ONHM bit in Register 5 enables a low-power ADC which digitizes the signal passed across the RNG1/2 pins. This signal is passed across the ISOcap link to the DSP. A current of approximately 450 µA is drawn from the line when this bit is activated. This mode is typically used to detect caller ID data. (See the “Caller ID” section.)

The on-hook line monitor can also be used to detect whether a phone line is physically connected to the

Si3014. If a line is present and the ONHM bit is set, SDO will have a near zero value and the LCS[3:0] bits will read 1111b. Due to the nature of the low-power ADC, the data presented on SDO could have up to a 10% dc offset.

If no line is connected, the output of SDO will move towards a negative full scale value (–32768). The value is guaranteed to be at least 89% of negative full scale. In addition, the LCS[3:0] bits will be zero.

Caller ID

The Si3034 provides the designer with the ability to pass caller ID data from the phone line to a caller ID decoder connected to the serial port.

In systems where the caller ID data is passed on the phone line between the first and second rings, the following method should be utilized to capture the caller ID data. The RDTP and RDTN register bits should be monitored to determine the completion of the first ring. After completion of the first ring, the DSP should set the SQLH bit (Register 18, bit 0) for a period of at least 1 ms. This resets the ac coupling network on the ring input in preparation for the caller ID data. The SQLH bit is then cleared, and the ONHM (Register 5, bit 3) should be asserted to enable the caller ID data to be passed to the DSP and presented on SDO. This bit enables a low-power ADC (approximately 450 µA is drawn from the line) which digitizes the signal passed across the RNG1/2 pins. This signal is passed across the ISOcap link to the DSP. The ONHM bit should be cleared after the caller ID data is received and prior to the second ring.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, the following method should be used to capture the caller ID data. The Si3034 supports both full- and half-wave rectified ring detection. Because a polarity reversal will trip either the RDTP or RDTN ring detection bits, the user must distinguish between a polarity reversal and a ring. This is accomplished using the full-wave ring detector in the device. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal. If it is a battery reversal, the DSP should set the SQLH bit (Register 18, bit 0) for a period of at least 1 ms. This resets the ac coupling network on the ring input in preparation for the caller ID data. The SQLH bit is then cleared, and the OHNM bit (Register 5, bit 3) should be asserted to enable the caller ID data to be passed to the DSP and presented on SDO. The ONHM bit should be cleared after the DSP has received the caller ID data.

Due to the nature of the low-power ADC, the data presented on SDO will have up to a 10% dc Offset. The caller ID decoder must either use a high pass or band pass filter to accurately retrieve the caller ID data.

Loop Current Monitor

It is desirable to have a measurement of the loop current being drawn from the line to determine if a telephone line is connected or if another telephone has picked up.

When the system is in an off-hook state, the LCS[3:0] bits in Register 12 indicate the dc loop current. An LCS[3:0] value of zero means the loop current is less than required for normal operation. When adequate loop current is available, the detector has 6 mA steps with a built-in hysteresis of 2 mA to provide stable LCS[3:0] values when near a transition. The LCS[3:0] value is a rough approximation of the loop current, and the designer is advised to use this value in a relative means rather than an absolute value. A typical LCS[3:0] transfer function is shown in Figure 22.

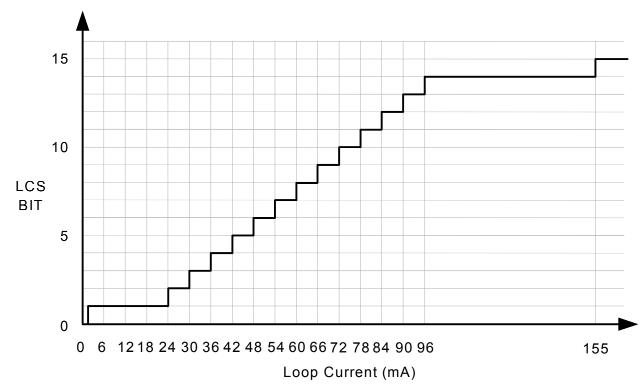


Figure 22. Typical LCS[3:0] Transfer Function

This feature enables the host processor to detect whether an additional line has “picked up” while the modem is transferring information. In the case of a second phone going off-hook, the loop current falls approximately 50% and is reflected in the value of the LCS[3:0] bits.

Overload Detection

The Si3034 can detect if an overload condition is present which may damage the DAA circuit. The DAA may be damaged if excessive line voltage or loop current is sustained.

In FCC and Japan dc termination modes, an LCS[3:0] value of 1111b means the loop current is greater than

155 mA indicating the DAA is drawing excessive loop current.

In CTR21 mode, 120 mA of loop current is not possible due to the current limit circuit. In this dc termination mode, an LCS[3:0] value of 1000b (8 decimal) or greater indicates an excessive loop current condition.

Analog Output

The Si3034 supports an analog output (AOUT) for driving the call progress speaker found with most of today's modems. AOUT is an analog signal that is comprised of a mix of the transmit and receive signals. The receive portion of this mixed signal has a 0 dB gain, while the transmit signal has a gain of –20 dB.

The transmit and receive signals of the AOUT signal have independent controls found in Register 6. The ATM[1:0] bits control the transmit portion, while the ARM[1:0] bits control the receive portion. The bits only affect the AOUT signal; they do not affect the modem data. Figure 17 on page 18 illustrates a recommended application circuit. In the configuration shown, the LM386 provides a gain of 26 dB. Additional gain adjustments may be made by varying the voltage divider created by R1 and R3.

Gain Control

The Si3034 supports multiple receive gain and transmit attenuation settings in Register 15. The receive path can support gains of 0, 3, 6, 9 and 12 dB, as selected with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. The transmit path can support attenuations of 0, 3, 6, 9 and 12 dB, as selected with the ATX[2:0] bits. The transmit path can also be muted with the TXM bit.

The gain control bits ARXB and ATXB in Register 13 are provided for firmware backwards compatibility with the Si3032 and Si3035 chipsets. These bits should be set to zero if the ARX[2:0] and ATX[2:0] in Register 15 are used.

Filter Selection

The Si3021 supports additional filter selections for the receive and transmit signals as defined in Table 11 and Table 12 on page 12. The IIRE bit in Register 16 selects between the IIR and FIR filters. The IIR filter provides a lower, but non-linear, group delay than the default FIR filter.

Clock Generation Subsystem

The Si3034 contains an on-chip clock generator. Using a single MCLK input frequency, the Si3034 can generate all the desired standard modem sample rates, as well as the common 11.025 kHz rate for audio playback.

The clock generator consists of two phase-locked loops (PLL1 and PLL2) that achieve the desired sample frequencies. Figure 23 illustrates the clock generator. The architecture of the dual PLL scheme allows for fast lock time on initial start-up, fast lock time when changing modem sample rates, high noise immunity, and the ability to change modem sample rates with a single register write. A large number of MCLK frequencies between 1 MHz and 60 MHz are supported. MCLK should be from a clean source, preferably directly from a crystal with a constant frequency and no dropped pulses.

In serial mode 2, the Si3021 operates as a slave device. The clock generator is configured (by default) to set the SCLK output equal to the MCLK input. The net effect is the clock generator multiplies the MCLK input by 20. For further details of slave mode operation, refer to "Multiple Device Support," on page 30.

Programming the Clock Generator

As noted in Figure 23, the clock generator must output a clock equal to 1024 • Fs, where Fs is the desired sample rate. The 1024 • Fs clock is determined through programming of the following registers:

Register 7: PLL1 N1[7:0] divider.

Register 8: PLL1 M1[7:0] divider.

Register 9: PLL2 N2[3:0] and M2[3:0] dividers.

Register 10: CGM Clock Generation Mode.

The main design consideration is the generation of a base frequency, defined as follows:

$$F_{BASE} = \frac{F_{MCLK} \cdot M1}{N1} = 36.864\,\text{MHz (CGM = 0)}$$

$$F_{BASE} = \frac{F_{MCLK} \cdot M1 \cdot 16}{N1 \cdot 25} = 36.864\,\text{MHz (CGM = 1)}$$

N1 (Register 7) and M1 (Register 8) are 8-bit unsigned values. F_{MCLK} is the frequency of the clock provided to the MCLK pin. Table 18 lists several standard crystal oscillator rates that could be supplied to MCLK. This list simply represents a sample of MCLK frequency choices. Many more are possible.

After PLL1 and the CGM bit have been programmed, PLL2 can be used to achieve all the standard modem sampling rates with a single write to Register 9. These standard sample rates are shown in Table 19. The values for N2 and M2 (Register 9) are shown in

Table 19. N2 and M2 are 4-bit unsigned values.

When programming the registers of the clock generator, the order of register writes is important. For PLL1 updates, N1 (Register 7) must always be written first, immediately followed by a write to M1 (Register 8). For PLL2, the CGM bit must be set as desired prior to writing N2 and M2 (Register 9). Changes to the CGM bit only take effect when N2 and M2 are written.

The values shown in Table 18 and Table 19 satisfy the equations above. However, when programming the registers for N1, M1, N2, and M2, the value placed in these registers must be one less than the value calculated from the equations. For example, for CGM = 0 with a MCLK of 48.0 MHz, the values placed in the N1 and M1 registers would be 0x7C and 0x5F, respectively. If CGM = 1, a non-zero value must be programmed to Register 9 in order for the 16/25 ratio to take effect.

PLL Lock Times

The Si3034 changes sample rates very quickly. However, lock time will vary based on the programming of the clock generator. The major factor contributing to PLL lock time is the CGM bit. When the CGM bit is used (set to 1), PLL2 will lock slower than when CGM is 0. The following relationships describe the boundaries on PLL locking time:

PLL1 lock time < 1 ms (CGM = 0,1)
PLL2 lock time 100 µs to 1 ms (CGM = 0)
PLL2 lock time <1 ms (CGM = 1)

For modem designs, it is recommended that PLL1 be programmed during initialization. No further programming of PLL1 is necessary. The CGM bit and PLL2 can be programmed for the desired initial sample rate, typically 7200 Hz. All further sample rate changes are made by simply writing to Register 9 to update PLL2.

The final design consideration for the clock generator is the update rate of PLL1. The following criteria must be satisfied in order for the PLLs to remain stable:

$$F_{UP1} = \frac{F_{MCLK}}{N1} \geq 144\ \text{KHz}$$

Where F_{UP1} is shown in Figure 23.

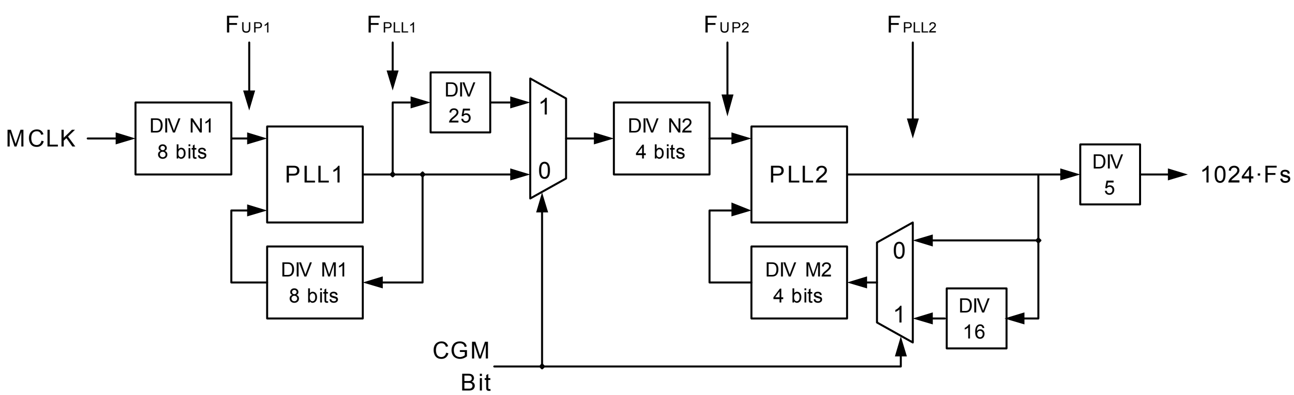


Figure 23. Clock Generation Subsystem

Table 18. MCLK Examples

MCLK (MHz)	N1	M1	CGM
1.8432	1	20	0
4.0000	5	72	1
4.0960	1	9	0
5.0688	11	80	0
6.0000	5	48	1
6.1440	1	6	0
8.1920	32	225	1
9.2160	1	4	0
10.0000	25	144	1
10.3680	9	32	0
11.0592	3	10	0
12.288	1	3	0
14.7456	2	5	0
16.0000	5	18	1
18.4320	1	2	0
24.5760	2	3	0
25.8048	7	10	0
33.8688	147	160	0
44.2368	96	125	1
46.0800	5	4	0
47.9232	13	10	0
48.0000	125	96	0
56.0000	35	36	1
60.0000	25	24	1

Table 19. N2, M2 Values (CGM = 0,1)

Fs (Hz)	N2	M2
7200	2	2
8000	9	10
8229	7	8
8400	6	7
9000	4	5
9600	3	4
10286	7	10

Setting Generic Sample Rates

The clock generation description focuses on the common modem sample rates. An application may require a sample rate not listed in Table 19, such as the common audio rate of 11.025 kHz. The restrictions and equations above still apply; however, a more generic relationship between MCLK and Fs (the desired sample rate) is needed. The following equation describes this relationship:

$$\frac{M1 \cdot M2}{N1 \cdot N2} = \text{ratio} \cdot \frac{5 \cdot 1024 \cdot Fs}{MCLK}$$

where Fs is the sample frequency, ratio = 1 for CGM = 0 and ratio = 25/16 for CGM = 1. All other symbols are shown in Figure 23.

By knowing the MCLK frequency and desired sample rate, the values for the M1, N1, M2, N2 registers can be determined. When determining these values, remember to consider the range for each register as well as the minimum update rate for the first PLL.

The values determined for M1, N1, M2, and N2 must be adjusted by –1 when determining the value written to the respective registers. This is due to internal logic, which adds 1 to the value stored in the register. This addition allows the user to write a 0 value in any of the registers and the effective divide by is 1. A special case occurs when both M1 and N1 and/or M2 and N2 are programmed with a 0 value. When Mx and Nx are both zero, the corresponding PLLx is bypassed. If M2 and N2 are set to 0, the ratio of 25/16 is eliminated and cannot be used in the above equation. In this condition the CGM bit has no effect.

Digital Interface

The Si3034 has two serial interface modes that support most standard modem DSPs. The M0 and M1 mode pins select the interface mode. The key difference between these two serial modes is the operation of the FSYNC signal. Table 20 summarizes the serial mode definitions.

Table 20. Serial Modes

Mode	M1 M0	Description
0	0 0	$\overline{\text{FSYNC}}$ frames data
1	0 1	$\overline{\text{FSYNC}}$ pulse starts data frame
2	1 0	Slave mode
3	1 1	Reserved

The digital interface consists of a single, synchronous serial link which communicates both telephony and control data.

In Serial mode 0 or 1, the Si3021 operates as a master, where the master clock (MCLK) is an input, the serial data clock (SCLK) is an output, and the frame sync signal (FSYNC) is an output. The MCLK frequency and the value of the sample rate control registers 7, 8, 9 and 10 determine the sample rate (Fs). The serial port clock, SCLK, runs at 256 bits per frame, where the frame rate is equivalent to the sample rate. Refer to "Clock Generation Subsystem," on page 27 for more details on programming sample rates.

The Si3034 transfers 16-bit or 15-bit telephony data in the primary timeslot and 16-bit control data in the secondary timeslot. Figure 24 and Figure 25 show the relative timing of the serial frames. Primary frames occur at the frame rate and are always present. To minimize overhead in the external DSP, secondary frames are present only when requested.

Two methods exist for transferring control information in the secondary frame. The default power-up mode uses the LSB of the 16-bit transmit (TX) data word as a flag to request a secondary transfer. In this mode, only 15-bit TX data is transferred, resulting in a loss of SNR but allowing software control of the secondary frames. As an alternative method, the FC pin can serve as a hardware flag for requesting a secondary frame. The external DSP can turn on the 16-bit TX mode by setting the SB bit in Register 1. In the 16-bit TX mode, the hardware FC pin must be used to request secondary transfers.

Figure 26 and Figure 27 illustrate the secondary frame read cycle and write cycle, respectively. During a read cycle, the R/W bit is high and the 5-bit address field contains the address of the register to be read. The contents of the 8-bit control register are placed on the SDO signal. During a write cycle, the R/W bit is low and the 5-bit address field contains the address of the register to be written. The 8-bit data to be written immediately follows the address on SDI. Only one register can be read or written during each secondary frame. See "Control Registers," on page 41 for the register addresses and functions.

In serial mode 2, the Si3021 operates as a slave device, where the MCLK is an input, the SCLK is a no connect (except for the master device for which it is an output), and the FSYNC is an input. In addition, the RGDT/FSD pin operates as a delayed frame sync (FSD) and the FC/RGDT pin operates as ring detect (RGDT). Note that in this mode, FC operation is not supported. For further details on operating the Si3021 as a slave device, refer to “Multiple Device Support.”

Multiple Device Support

The Si3034 supports the operation of up to 7 additional devices on a single serial interface. Figure 32 shows the typical connection of the Si3034 and one additional serial voice codec (Si3000).

The Si3034 must be the master in this configuration. The secondary codec should be configured as a slave device with SCLK and FSYNC as inputs. On power up, the Si3034 master will be unaware of the additional codec on the serial bus. The FC/RGDT pin is an input, operating as the hardware control for secondary frames, and the RGDT/FSD pin is an output, operating as the active low ring detection signal. The master device should be programmed for master/slave mode prior to enabling the ISOcap link, because a ring signal would cause a false transition to the slave device’s FSYNC.

Register 14 provides the necessary control bits to configure the Si3034 for master/slave operation. Bit 0 (DCE) sets the Si3034 in master/slave mode, also referred to as daisy-chain mode. When the DCE bit is set, the FC/RGDT pin becomes the ring detect output and the RGDT/FSD pin becomes the frame sync delay output.

Bits 7:5 (NSLV2:NSLV0) set the number of slaves to be supported on the serial bus. For each slave, the Si3034 will generate a FSYNC to the DSP. In daisy-chain mode, the polarity of the ring signal can be controlled by bit 1 (RPOL). When RPOL = 1, the ring detect signal (now output on the FC/RGDT pin) is active high.

The Si3034 supports a variety of codecs as well as additional Si3034s. The type of slave codec(s) used is set by bits 4:3 (SSEL1:SSEL0). These bits determine the type of signalling used in the LSB of SDO. This assists the DSP in isolating which data stream is the master and which is the slave. If the LSB is used for signalling, the master device will have a unique setting relative to the slave devices. The DSP can use this information to determine which FSYNC marks the beginning of a sequence of data transfers.

The delayed frame sync (FSD) of each device is supplied as the FSYNC of each subsequent slave device in the daisy chain. The master Si3034 will generate an FSYNC signal for each device every 16 or 32 SLCK periods. The delay period is set by Register 14, bit 2 (FSD). Figures 28–31 show the relative timing for daisy chaining operation. Note that primary communication frames occur in sequence, followed by secondary communication frames, if requested. When writing/reading the master device via a secondary frame, all secondary frames of the slave devices must be written as well. When writing/reading a slave device via a secondary frame, the secondary frames of the master and all other slaves must be written as well. "No operation" writes/reads to secondary frames are accomplished by writing/reading a zero value to address zero.

If FSD is set for 16 SCLK periods between $\overline{\text{FSYNC}}$s, only serial mode 1 can be used. In addition, the slave devices must delay the tri-state to active transition of their SDO sufficiently from the rising edge of SCLK to avoid bus contention.

The Si3034 supports the operation of up to eight Si3034 devices on a single serial bus. The master Si3034 must be configured in serial mode 1. The slave(s) Si3034 is configured in serial mode 2. Figure 33 on page 40 shows a typical master/slave connection using three Si3034 devices.

When in serial mode 2, $\overline{\text{FSYNC}}$ becomes an input, $\overline{\text{RGDT}}$/FSD becomes the delay frame sync output, and FC/$\overline{\text{RGDT}}$ becomes the ring detection output. In addition, the internal PLLs are fixed to a multiply by 20. This provides the desired sample rate when the master's SCLK is provided to the slave's MCLK. Note that the SCLK of the slave is a no connect in this configuration.

The delay between $\overline{\text{FSYNC}}$ input and delayed frame sync output ($\overline{\text{RGDT}}$/FSD) will be 16 SCLK periods. The $\overline{\text{RGDT}}$/FSD output has a waveform identical to the $\overline{\text{FSYNC}}$ signal in serial mode 0. In addition, the LSB of SDO is set to zero by default for all devices in serial mode 2.

Power Management

The Si3034 supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full power down mode. The power management modes are controlled by the PDN and PDL bits in Register 6.

On power up, or following a reset, the Si3034 is in reset operation. In this mode, the PDL bit is set, while the PDN bit is cleared. The Si3021 is fully operational, except for the ISOcap link. No communication between the Si3021 and Si3014 can occur during reset operation. Any bits associated with the Si3014 are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The Si3021 is fully operational and the ISOcap link is passing information between the Si3021 and the Si3014. The clock generator must be programmed to a valid sample rate prior to entering this mode.

The Si3034 supports a low-power sleep mode. This mode supports the popular wake-up-on-ring feature of many modems. The clock generator registers 7, 8, and 9 must be programmed with valid non-zero values prior to enabling sleep mode. Then, the PDN bit must be set and the PDL bit cleared. When the Si3034 is in sleep mode, the MCLK signal may be stopped or remain active, but it *must* be active before waking up the Si3034. The Si3021 is non-functional except for the ISOcap and $\overline{\text{RGDT}}$ signal. To take the Si3034 out of sleep mode, pulse the reset pin ($\overline{\text{RESET}}$) low.

In summary, the power down/up sequence for sleep mode is as follows:

1. Registers 7, 8, and 9 must have valid non-zero values.
2. Set the PDN bit (Register 6, bit 3) and clear the PDL bit (Register 6, bit 4).
3. MCLK may stay active or stop.
4. Restore MCLK before initiating the power-up sequence.
5. Reset the Si3034 using $\overline{\text{RESET}}$ pin (after MCLK is present).
6. Program registers to desired settings.

The Si3034 also supports an additional power-down mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) are set, the chipset enters a complete power-down mode and draws negligible current (deep sleep mode). PLL2 should be turned off prior to entering deep sleep mode (i.e., set Register 9 to 0 and then Register 6 to 0x18). In this mode, the $\overline{\text{RGDT}}$ pin does not function. Normal operation may be restored using the same process for taking the chipset out of sleep mode.

Calibration

The Si3034 initiates an auto-calibration by default whenever the device goes off-hook or experiences a loss in line power. Calibration is used to remove any offsets that may be present in the on-chip A/D converter which could affect the A/D dynamic range. Auto-calibration is typically initiated after the DAA dc termination stabilizes, and takes 512/Fs seconds to complete. Due to the large variation in line conditions and line card behavior that can be presented to the DAA, it may be beneficial to use manual calibration in lieu of auto-calibration.

Manual calibration should be executed as close to 512/Fs seconds before valid transmit/receive data is expected.

The following steps should be taken to implement manual calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to one and then zero to begin and complete the calibration.
3. The calibration will be completed in 512/Fs seconds.

In-Circuit Testing

The Si3034's advanced design provides the modem manufacturer with increased ability to determine system functionality during production line tests, as well as support for end-user diagnostics. Four loopback modes exist allowing increased coverage of system components. For three of the test modes, a line-side power source is needed. While a standard phone line can be used, the test circuit in Figure 1 on page 5 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side chip.

For the start-up test mode, no line-side power is necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line side is in a power-down mode and the DSP side is in a digital loop-back mode. In this mode, data received on SDI is passed through the internal filters and transmitted on SDO. This path will introduce approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters will exist between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line side. When PDL is cleared the FDT bit (Register 12, bit 6) will become active, indicating the successful communication between the line side and DSP side. This can be used to verify that the ISOcap is operational.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirement:

1. Power up or reset.
2. Program clock generator to desired sample rate.
3. Enable line-side by clearing PDL bit.
4. Issue off-hook.
5. Delay 1548/Fs sec to allow calibration to occur.
6. Set desired test mode.

The ISOcap digital loopback mode allows the data pump to provide a digital input test pattern on SDI and receive that digital test pattern back on SDO. To enable this mode, set the DL bit in Register 1. In this mode, the isolation barrier is actually being tested. The digital stream is delivered across the isolation capacitor, C1 of Figure 16 on page 15, to the line-side device and returned across the same barrier. In this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive a signal on the telephone line into the Si3034 line-side device and have it driven back out onto the line. This mode allows testing of external components connecting the RJ-11 jack (TIP and RING) to the Si3014. To enable this mode, set the AL bit in Register 2.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side chip and the external components in Figure 16 on page 15. In this test mode, the data pump provides a digital test waveform on SDI. This data is passed across the isolation barrier, transmitted to and received from the line, passed back across the isolation barrier, and presented to the data pump on SDO. To enable this mode, clear the HBE bit in Register 2.

When the HBE bit is cleared, this will cause a dc offset which affects the signal swing of the transmit signal. In this test mode, it is recommended that the transmit signal be 12 dB lower than normal transmit levels. This lower level will eliminate clipping caused by the dc offset which results from disabling the hybrid. It is assumed in this test that the line ac impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

Exception Handling

The Si3034 provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling DSP can read several status bits. The bit of highest importance is the frame detect bit (FDT, Register 12, bit 6). This bit indicates that the DSP-side (Si3021) and line-side (Si3014) devices are communicating. During normal operation, the FDT bit can be checked before reading any bits that indicate information about the line side. If FDT is not set, the following bits related to the line-side are invalid—RDT, RDTN, RDTP, LCS[3:0], CBID, REVB[3:0], CTRO, and OVL; the $\overline{\text{RGDT}}$ operation will also be non-functional.

Following power-up and reset, the FDT bit is not set because the PDL bit (Register 6, bit 4) defaults to 1. In this state, the ISOcap link is not operating and no information about the line-side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the ISOcap link. While the DSP and line side are establishing communication, the DSP-side does not generate $\overline{\text{FSYNC}}$ signals. Establishing communication will take less than 10 ms. Therefore, if the controlling DSP serial interface is interrupt driven, based on the $\overline{\text{FSYNC}}$ signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit can also indicate if the line-side executes an off-hook request successfully. If the line-side is not connected to a phone line (i.e., the user fails to connect a phone line to the modem), the FDT bit remains cleared. The controlling DSP must allow sufficient time for the line-side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT is high, the LCS[3:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit in Register 6 must be set high for at least 1 ms to reset the line side.

Another useful bit is the communication link error (CLE) bit (Register 12, bit 7). The CLE bit indicates a time-out error for the ISOcap link following a change to either PLL1 or PLL2. When the CLE bit is set, the DSP-side chip has failed to receive verification from the line-side that the clock change has been accepted in an expected period of time (less than 10 ms). This condition indicates a severe error in programming the clock generator or possibly a defective line-side chip.

Revision Identification

The Si3034 provides the system designer the ability to determine the revision of the Si3021 and/or the Si3014. The REVA[3:0] bits in Register 11 identify the revision of the Si3021. The REVB[3:0] and CBID bits in Register 13 identify the revision of the Si3014.

Table 21. Revision Values

Revision	Si3021	Si3014
A	1000	0001
B	1001	0010
C	1010	0011

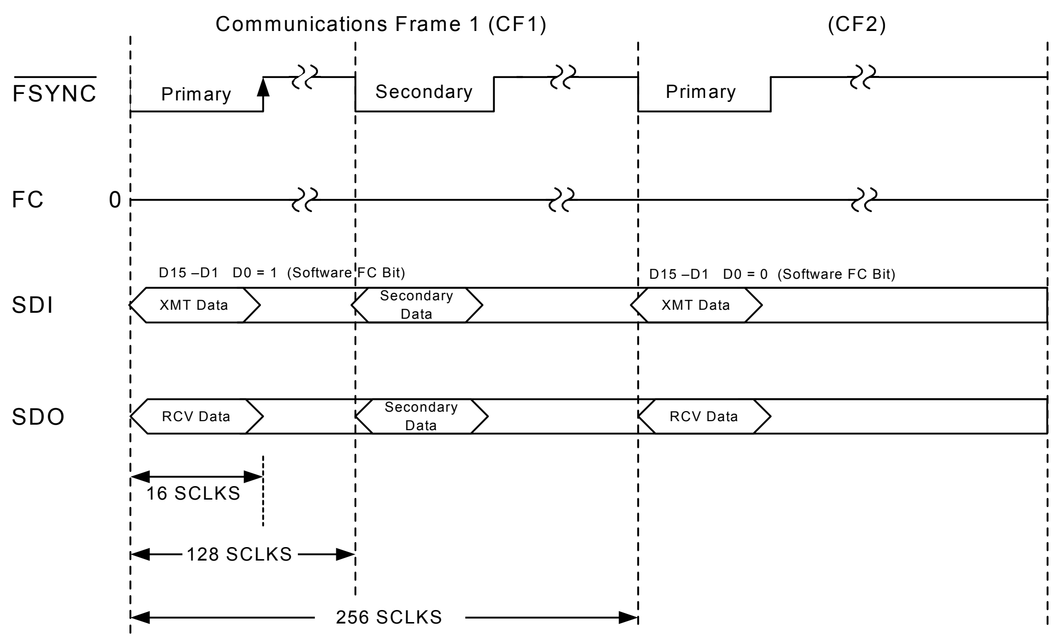


Figure 24. Software FC/$\overline{\text{RGDT}}$ Secondary Request

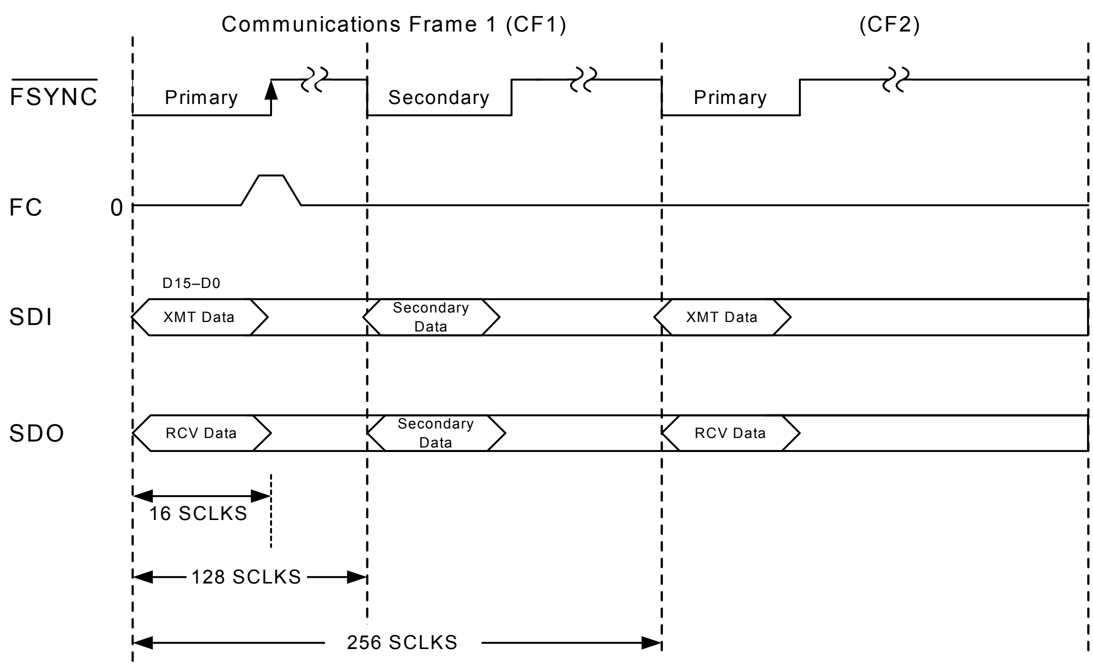


Figure 25. Hardware FC/$\overline{\text{RGDT}}$ Secondary Request

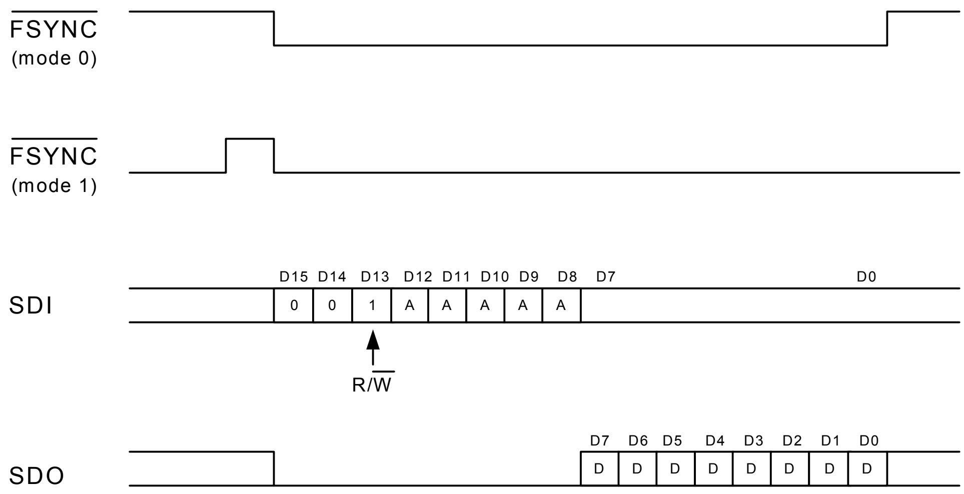


Figure 26. Secondary Communication Data Format—Read Cycle

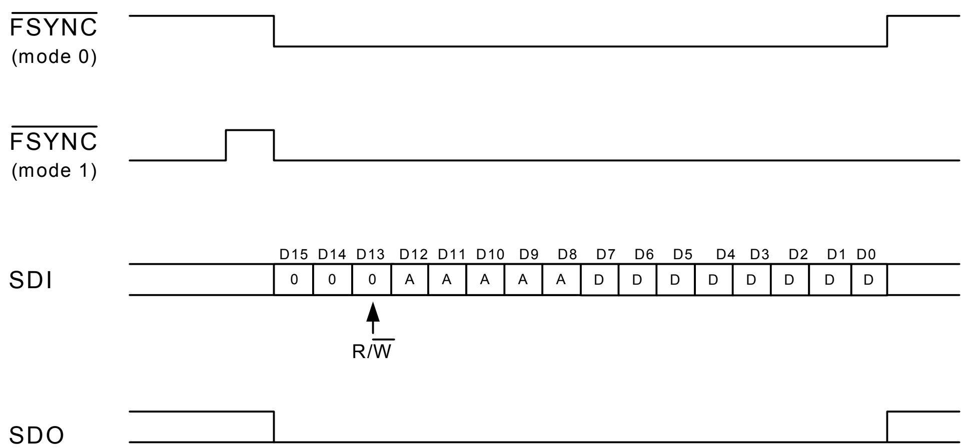


Figure 27. Secondary Communication Data Format—Write Cycle

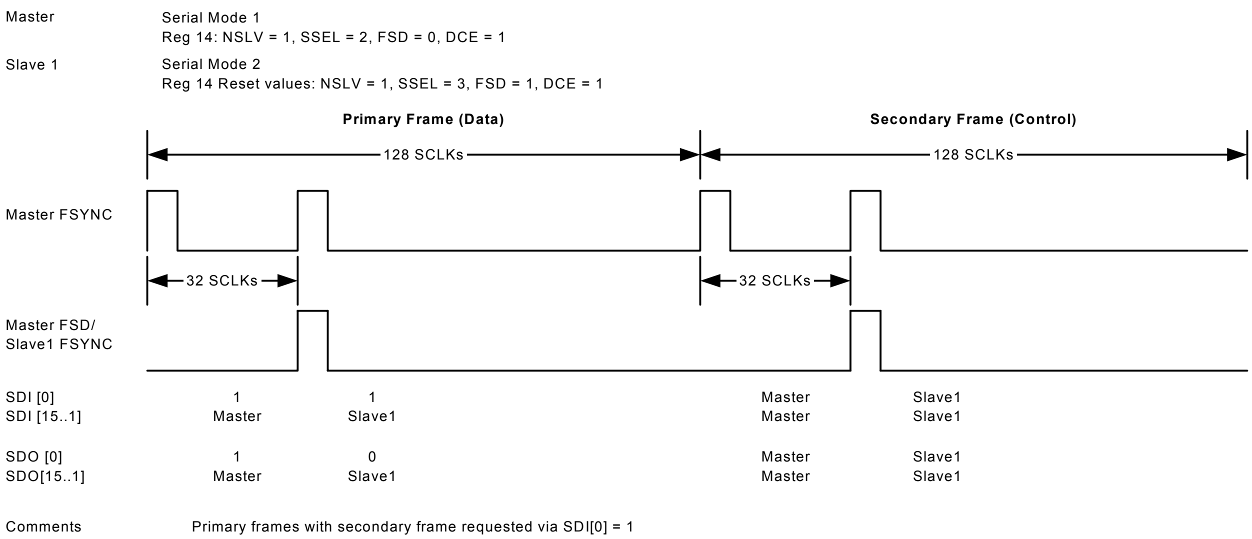


Figure 28. Daisy Chaining of a Single Slave (Pulse FSD)

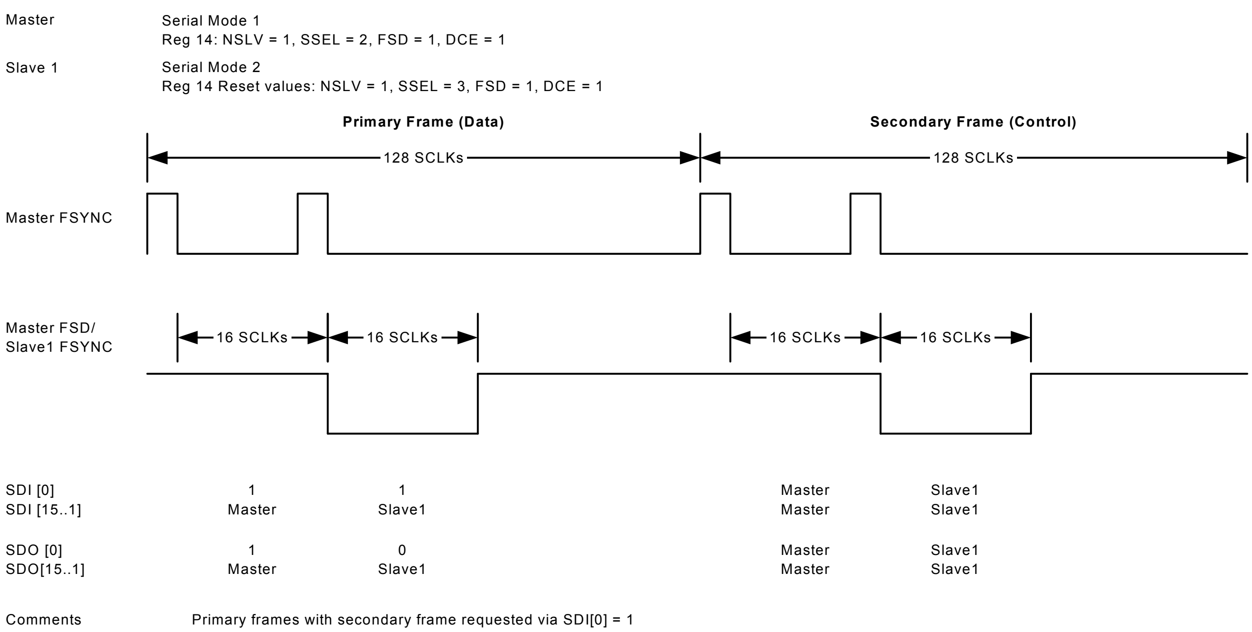


Figure 29. Daisy Chaining of a Single Slave (Frame FSD)

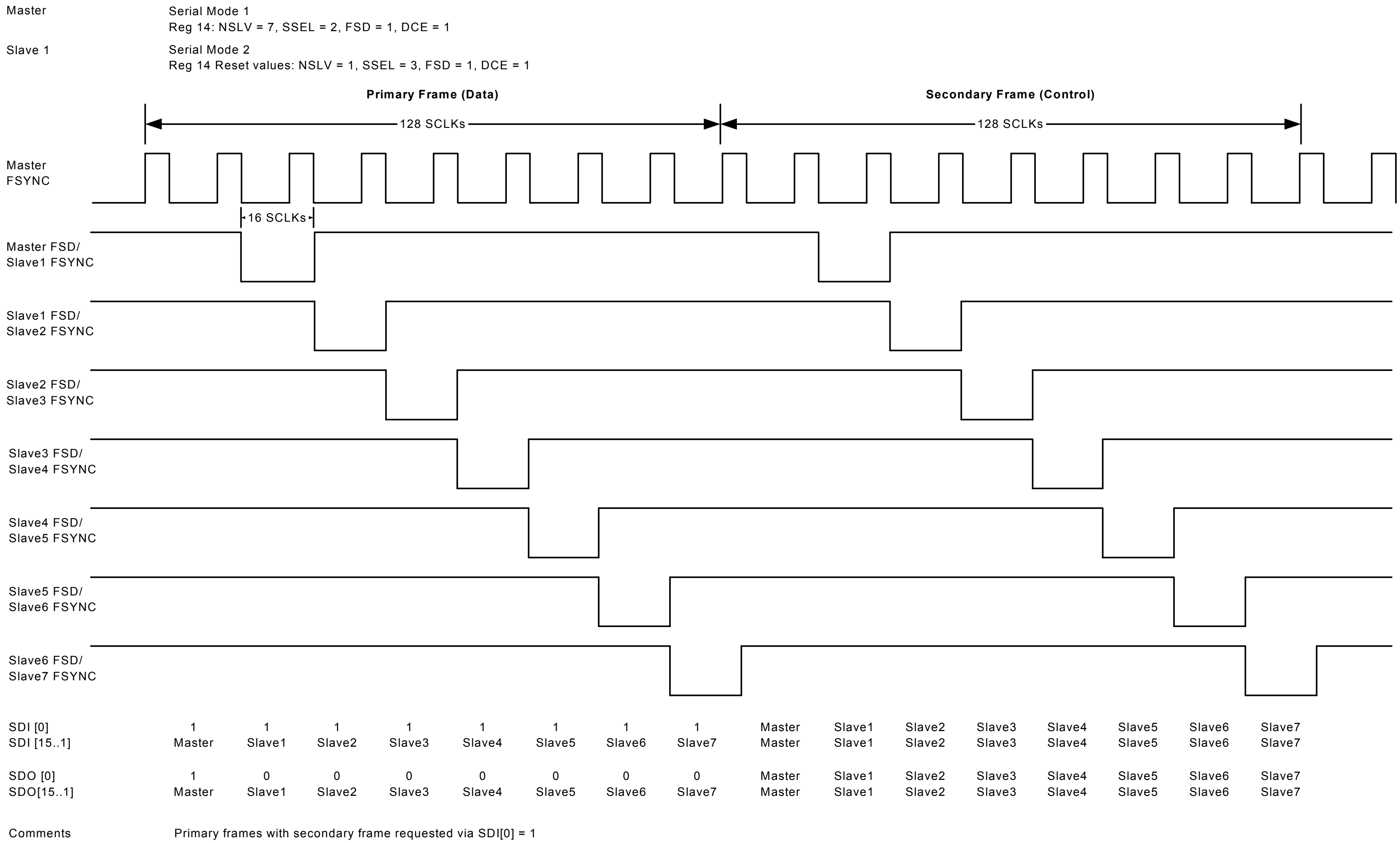


Figure 30. Daisy Chaining of Eight DAAs

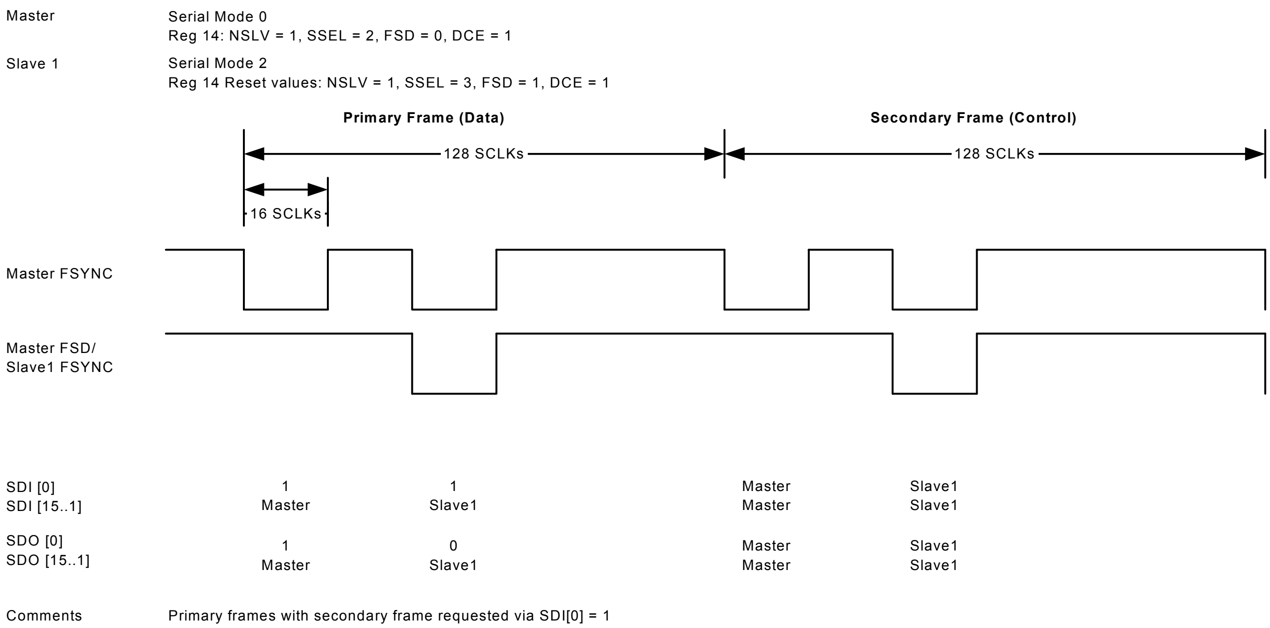


Figure 31. Daisy Chaining with Framed FSYNC and Framed FSD

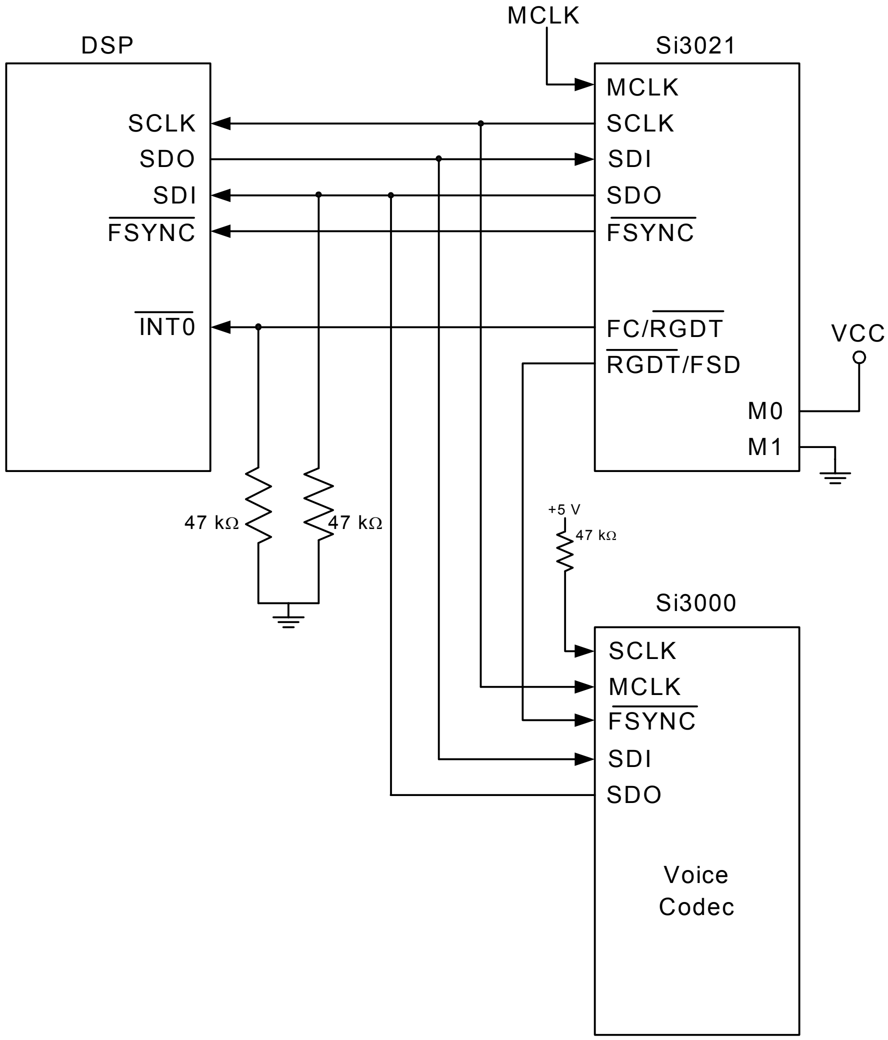


Figure 32. Typical Connection for Master/Slave Operation (e.g, Data/Fax/Voice Modem)

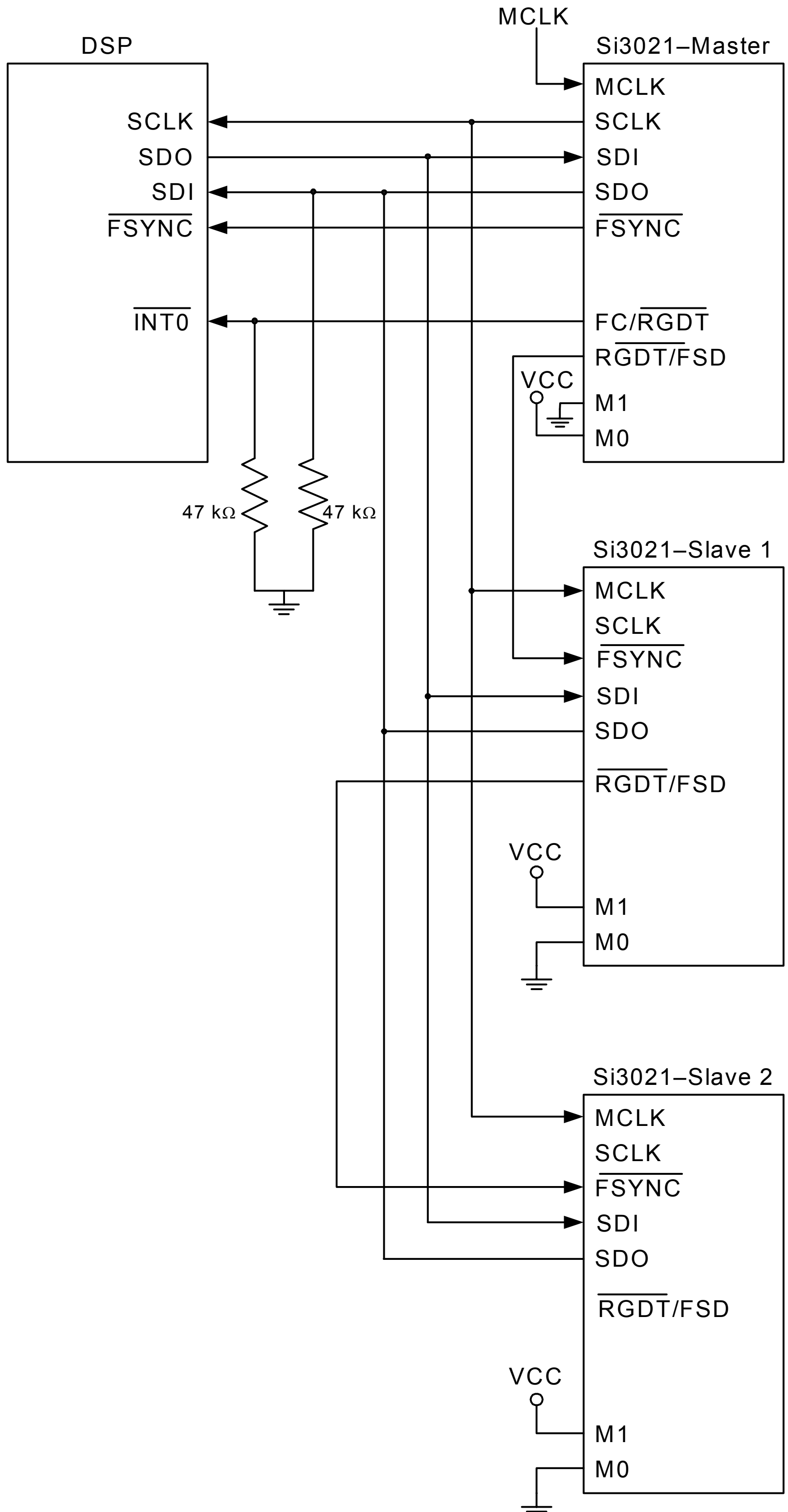


Figure 33. Typical Connection for Multiple Si3034s

Control Registers

Note: Any register not listed here is reserved and should not be written.

Table 22. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR						DL	SB
2	Control 2					AL		HBE	RXE
3	Reserved								
4	Reserved								
5	DAA Control 1		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
6	DAA Control 2	CPE	ATM[1]	ARM[1]	PDL	PDN		ATM[0]	ARM[0]
7	PLL1 Divide N1	N1[7:0]							
8	PLL1 Divide M1	M1[7:0]							
9	PLL2 Divide/Multiply N2/ M2	N2[3:0]				M2[3:0]			
10	PLL Control								CGM
11	Chip A Revision					REVA[3:0]			
12	Line Side Status	CLE	FDT			LCS[3:0]			
13	Chip B Revision		CBID	REVB[3:0]				ARXB	ATXB
14	Daisy Chain Control	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
15	TX/RX Gain Control	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	International Control 1		OHS	ACT	IIRE	DCT[1:0]		RZ	RT
17	International Control 2		MCAL	CALD	LIM[1:0]		BTE	ROV	BTD
18	International Control 3		DIAL	FJM	VOL[1:0]			RFWE	SQLH
19	International Control 4						OVL		

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR						DL	SB
Type	R/W						R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset**. 0 = Enables chip for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit will automatically clear after being set.
6:2	Reserved	Read returns zero.
1	DL	**Isolation Digital Loopback**. 0 = Digital loopback across the isolation barrier disabled. 1 = Enables digital loopback mode across the isolation barrier. The line-side must be enabled prior to setting this mode.
0	SB	**Serial Digital Interface Mode**. 0 = Operation is in 15-bit mode, and the LSB of the data field indicates whether a secondary frame is required. 1 = The serial port is operating in 16-bit mode and requires use of the secondary frame sync signal (FC) to initiate control data reads/writes.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					AL		HBE	RXE
Type					R/W		R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	AL	**Analog Loopback**. 0 = Analog loopback mode disabled. 1 = Enables external analog loopback mode.
2	Reserved	Read returns zero.
1	HBE	**Hybrid Enable**. 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable**. 0 = Receive path disabled. 1 = Enables receive path.

Register 3. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 4. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP	OPOL	ONHM	RDT	OHE	OH
Type		R	R	R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	OPOL	**Off-Hook Polarity**. 0 = Off-hook pin is active low. 1 = Off-hook pin is active high.
3	ONHM	**On-Hook Line Monitor**. 0 = Normal on-hook mode. 1 = Enables low-power monitoring mode allowing the DSP to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect**. 0 = Reset either 4.5–9 seconds after last positive ring is detected or when the system executes an off-hook. 1 = Indicates a ring is occurring.
1	OHE	**Off-Hook Pin Enable**. 0 = Off-hook pin is ignored. 1 = Enables the operation of the off-hook pin.
0	OH	**Off-Hook**. 0 = Line-side device is on-hook. 1 = Causes the line-side chip to go off-hook. This bit operates independently of the OHE bit and is a logic OR with the off-hook pin when enabled.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPE	ATM[1]	ARM[1]	PDL	PDN		ATM[0]	ARM[0]
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0111_0000

Bit	Name	Function
7	CPE	**Charge Pump Enable**. 0 = Charge pump is disabled. 1 = Charge pump is enabled. If the charge pump is not to be enabled, R3 must be installed with 10 Ω, 1/10W and V_D must be between 4.75 and 5.25 V.
6,1	ATM[1:0]	**AOUT Transmit Path Level Control**. 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –32 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
5,0	ARM[1:0]	**AOUT Receive Path Level Control.** 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
4	PDL	**Power Down Line-Side Chip.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the Si3014 in lower power mode.
3	PDN	**Power Down.** 0 = Normal operation. 1 = Powers down the Si3021. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2	Reserved	Read returns zero.

Register 7. PLL1 Divide N1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1, 2)

Bit	Name	Function
7:0	N1[7:0]	**PLL N1 Divider**. Contains the (value – 1) for determining the output frequency on PLL1.

Register 8. PLL1 Multiply M1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	M1							
Type	R/W							

Reset settings = 0000_0000 (serial mode 0, 1)

Reset settings = 0001_0011 (serial mode 2)

Bit	Name	Function
7:0	M1[7:0]	**PLL1 M1 Multiplier**. Contains the (value – 1) for determining the output frequency on PLL1.

Register 9. PLL2 Divide/Multiply N2/M2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2				M2			
Type	R/W				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7:4	N2[3:0]	**PLL2 N2 Divider.** Contains the (value – 1) for determining the output frequency on PLL2.
3:0	M2[3:0]	**PLL2 M2 Multiplier.** Contains the (value – 1) for determining the output frequency on PLL2.

Register 10. PLL Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								CGM
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	reserved	Read returns zero.
0	CGM	**Clock Generation Mode**. 0 = No additional ratio is applied to the PLL and faster lock times are possible. 1 = A 25/16 ratio is applied to the PLL allowing for a more flexible choice of MCLK frequencies while slowing down the PLL lock time.

Register 11. Chip A Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					REVA[3:0]			
Type	R							

Reset settings = N/A

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	REVA[3:0]	**Chip A Revision**. Four-bit value indicating the revision of the Si3021 (DSP-side) chip.

Register 12. Line-Side Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLE	FDT			LCS[3:0]			
Type	R/W	R				R		

Reset settings = N/A

Bit	Name	Function
7	CLE	**Communications (ISOcap link) Error**. 0 = ISOcap communication link between the Si3021 and the Si3014 is operating correctly. 1 = Indicates a communication problem between the Si3021 and the Si3014. When it goes high, it remains high until a logic 0 is written to it.
6	FDT	**Frame Detect**. 0 = Indicates ISOcap link has not established frame lock. 1 = Indicates ISOcap link frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	LCS[3:0]	**Loop Current Sense**. Four-bit value returning the loop current in 6 mA increments. 0 = Loop current < 0.4 mA typical. 1111 = Loop current > 155 mA typical. See “Loop Current Monitor” section.

Register 13. Chip B Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CBID	REVB[3:0]				ARXB	ATXB
Type		R	R				R/W	R/W

Reset settings = N/A

Bit	Name	Function
7	Reserved	Read returns zero.
6	CBID	**Chip B ID**. 0 = Indicates the line-side is domestic only. 1 = Indicates the line-side has international support.
5:2	REVB[3:0]	**Chip B Revision**. Four-bit value indicating the revision of the Si3014 (line-side) chip.
1	ARXB	**Receive Gain**. 0 = 0 dB gain is applied to the receive path. 1 = A 6 dB gain is applied to the receive path. **Note:** This bit is for Si3032 backwards compatibility. The Si3034 has additional receive gain settings ARX[2:0] in Register 15. ARXB should be set to 0 if the settings in Register 15 are used.
0	ATXB	**Transmit Attenuation**. 0 = 0 dB gain is applied to the transmit path. 1 = A 3 dB attenuation is applied to the transmit path. **Note:** This bit is for Si3032 backwards compatibility. The Si3034 has additional transmit gain settings ATX[2:0] in Register 15. ATXB should be set to 0 if the settings in Register 15 are used.

Register 14. Daisy Chain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NSLV[2:0]			SSEL[1:0]		FSD	RPOL	DCE
Type	R/W			R/W		R/W	R/W	R/W

Reset settings = 0000_0010 (serial mode 0,1)

Reset settings = 0011_1111 (serial mode 2)

Bit	Name	Function
7:5	NSLV[2:0]	**Number of Slave Devices.** 000 = 0 slaves. Simply redefines the FC/$\overline{\text{RGDT}}$ and $\overline{\text{RGDT}}$/FSD pins. 001 = 1 slave device 010 = 2 slave devices 011 = 3 slave devices 100 = 4 slave devices (For four or more slave devices, the FSD bit MUST be set.) 101 = 5 slave devices 110 = 6 slave devices 111 = 7 slave devices
4:3	SSEL[1:0]	**Slave Device Select.** 00 = 16-bit SDO receive data 01 = Reserved 10 = 15-bit SDO receive data. LSB = 1 for the Si3034 device. 11 = 15-bit SDO receive data. LSB = 0 for the Si3034 device.
2	FSD	**Delayed Frame Sync Control.** 0 = Sets the number of SCLK periods between frame syncs to 32. 1 = Sets the number of SCLK periods between frame syncs to 16. This bit **MUST** be set when Si3034 devices are slaves. For the master Si3034, only serial mode 1 is allowed in this case.
1	RPOL	**Ring Detect Polarity.** 0 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active low. 1 = The FC/$\overline{\text{RGDT}}$ pin (operating as ring detect) is active high.
0	DCE	**Daisy-Chain Enable.** 0 = Daisy-chaining disabled. 1 = Enables the Si3034 to operate with slave devices on the same serial bus. The FC/$\overline{\text{RGDT}}$ signal (pin 7) becomes the ring detect output and the $\overline{\text{RDGT}}$/FSD signal (pin 15) becomes the delayed frame sync signal. **ALL** other bits in this register are ignored if DCE = 0.

Register 15. TX/RX Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation **Note:** Register 13 ATXB bit must be 0 if these bits are used.
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain.** 000 = 0 dB gain 001 = 3 dB gain 010 = 6 dB gain 011 = 9 dB gain 1xx = 12 dB gain **Note:** Register 13 ARXB bit must be 0 if these bits are used.

Register 16. International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		OHS	ACT	IIRE	DCT[1:0]		RZ	RT
Type		R/W	R/W	R/W	R/W		R/W	R/W

Reset settings = 0000_1000

Bit	Name	Function
7	Reserved	Read returns zero.
6	OHS	**On-Hook Speed.** 0 = The Si3034 will execute a fast on-hook. 1 = The Si3034 will execute a slow, controlled on-hook.
5	ACT	**AC Termination Select.** 0 = Selects the real impedance. 1 = Selects the complex impedance.
4	IIRE	**IIR Filter Enable.** 0 = FIR filter enabled for transmit and receive filters. (See Figures 6–9 on page 13.) 1 = IIR filter enabled for transmit and receive filters. (See Figures 10–15 on page 14.)
3:2	DCT[1:0]	**DC Termination Select.** 00 = Reserved 01 = Japan Mode. Low voltage mode. (Transmit level = –3 dBm). 10 = FCC Mode. Standard voltage mode. (Transmit level = –1 dBm). 11 = CTR21 Mode. Current limiting mode. (Transmit level = –1 dBm).
1	RZ	**Ringer Impedance**. 0 = Maximum (high) ringer impedance. 1 = Synthesized ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See "Ringer Impedance," on page 24.
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level will not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. 0 = 11 to 22 V_{RMS} 1 = 17 to 33 V_{RMS}

Register 17. International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MCAL	CALD	LIM[1:0]		BTE	ROV	BTD
Type		R/W	R/W	R/W		R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Must be zero.
6	MCAL	**Manual Calibration.** 0 = No calibration. 1 = Initiate calibration.
5	CALD	**Auto-Calibration Disable.** 0 = Auto-calibration enabled. 1 = Auto-calibration disabled.
4:3	LIM[1:0]	**Current Limit.** 00 = All other modes. 11 = CTR21 mode.
2	BTE	**Billing Tone Detect Enable.** 0 = Billing tone detection disabled. 1 = Billing tone detection enabled. When set, the Si3034 can detect a billing tone signal on the line and maintain off-hook through the billing tone. If a billing tone is detected, the BTD bit in Register 17 will be set to indicate the event.
1	ROV	**Receive Overload.** 0 = Normal receive input level. 1 = Excessive receive input level. This bit is set if the BTE bit in Register 17 is enabled and the RX pin has an excessive input level. This bit is cleared by writing a 0 to this location.
0	BTD	**Billing Tone Detected.** 0 = No billing tone detected. 1 = Billing tone detected. This bit will be set if the BTE bit in Register 17 is enabled and a billing tone is detected. This bit is cleared by writing a 0 to this location.

Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DIAL	FJM	VOL[1:0]			RFWE	SQLH
Type		R/W	R/W	R/W			R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	DIAL	**DTMF Dialing Mode.** This bit should be set during DTMF dialing in CTR21 mode if LCS[3:0] < 6. 0 = Normal operation. 1 = Increase headroom for DTMF dialing.
5	FJM	**Force Japan DC Termination Mode.** 0 = Normal Gain. 1 = When Register 16, DCT[1:0], is set to 10b (FCC mode), setting this bit will force Japan dc termination mode while allowing for a transmit level of –1 dBm. See “DTMF Dialing” on page 24.
4:3	VOL[1:0]	**Line Voltage Adjust.** When set, this bit will adjust the TIP-RING line voltage. Lowering this voltage will improve margin in low voltage countries. Raising this voltage may improve distortion performance. 00 = Normal 01 = –0.125 V 10 = 0.25 V 11 = 0.125 V
2	Reserved	Read returns zero.
1	RFWE	**Ring Detector Full Wave Rectifier Enable.** When set, the ring detection circuitry provides full-wave rectification. This will affect the $\overline{\text{RGDT}}$ pin as well as the data stream presented on SDO during ring detection. 0 = Half Wave. 1 = Full Wave.
0	SQLH	**Ring Detect Network Squelch.** This bit must be set, then cleared after at least 1 ms, following a polarity reversal or ring signal detection. It is used to quickly recover the offset on the RNG1/2 pins after a polarity reversal or ring signal. 0 = Normal operation. 1 = Squelch function is enabled.

Register 19. International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL		
Type						R		

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read may return zero or one.
6:3	Reserved	Read returns zero.
2	OVL	**Overload Detected.** 0 = Normal receive input level. 1 = Excessive receive input level. This bit has the same function as ROV in Register 17, but will clear itself after the overload has been removed. See “Billing Tone Detection” on page 24. This bit is only functional when the BTE bit in Register 17 is enabled.
1:0	Reserved	Read returns zero.

APPENDIX A—UL1950 3RD EDITION

Although designs using the Si3034 comply with UL1950 3rd Edition and pass all overcurrent and overvoltage tests, there are still several issues to consider.

Figure 34 shows two designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 34 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 34 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests will apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.

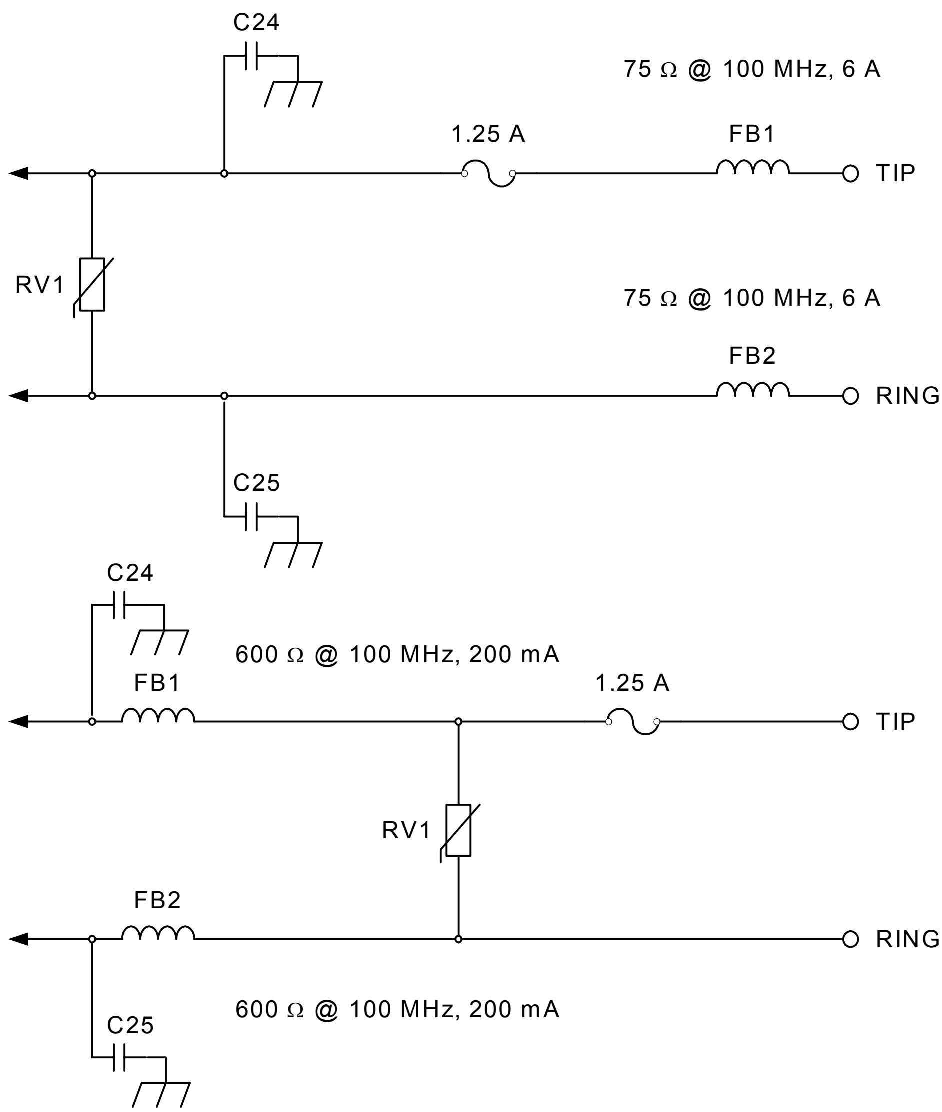


Figure 34. Circuits that Pass all UL1950 Overvoltage Tests

APPENDIX B—CISPR22 COMPLIANCE

Various countries are expected to adopt the IEC CISPR22 standard over the next few years. For example, the European Union (EU) has adopted a standard entitled EN55022, which is based on the CISPR22 standard. EN55022 is now part of the EU's EMC Directive and compliance is expected to be required starting in 2003. Adherence to this standard will be necessary to display the CE mark on designs intended for sale in the EU. The typical schematic and global bill of materials (BOM) (see Figure 16 and Table 13) contained in this data sheet are designed to be compliant to the CISPR22 standard.

If smaller inductors are desired, a notch filter may be used and compliance to CISPR22 still achieved. As shown in Figure 35, a series capacitor-resistor in parallel with L1 and L2 forms the simple notch filter. Table 23 shows corresponding values used for C24, C25, C38, C39, L1, L2, R31, and R32.

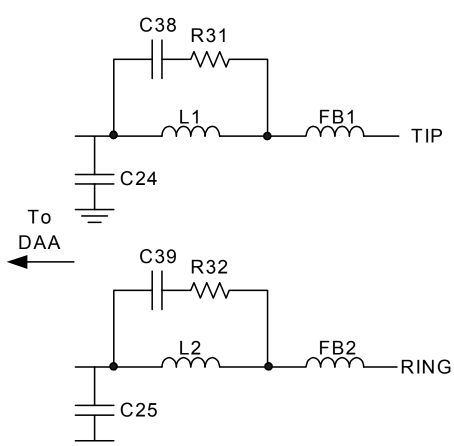


Figure 35. Notch Filter for CISPR22 Compliance

Table 23. Notch Filter Component Values

C24/C25	C38/C39	L1/L2	R31/R32
1000 pF	33 pF, 50 V	150 µH, DCR < 3 Ω, I > 120 mA	680 Ω, 1/10 W

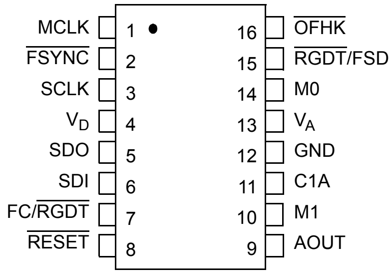
The direct current resistance (DCR) of the listed inductors is an important consideration. If the DCR of the inductors used is less than 3 Ω each, then country PTT specifications which require 300 Ω or less of dc resistance at TIP and RING with 20 mA of loop current can be satisfied with the Japan dc termination mode. If the DCR of the inductors is at or slightly above 3 Ω, the low voltage termination mode may need to be used to satisfy the 300 Ω dc resistance requirement at 20 mA of loop current. In all cases, "DC Termination Considerations," on page 23 should be followed.

If compliance to the CISPR22 standard and certain other country PTT requirements are not desired, then L1 and L2 may be removed. If these inductors are removed, C24 and C25 should be increased to 2200 pF, and C9 should be changed to 22 nF, 250 V. With these changes, PTT compliance in the following countries will not be achieved: India (I/Fax-03/03 standard), Taiwan (ID0001 standard), Chile (Decree No. 220 1981 standard), and Argentina (CNC-St2-44.01 standard).

For questions concerning compliance to CISPR22 or other relevant standards, contact a Silicon Laboratories technical representative.

Pin Descriptions: Si3021

Si3021 (SOIC)



Si3021 (TSSOP)

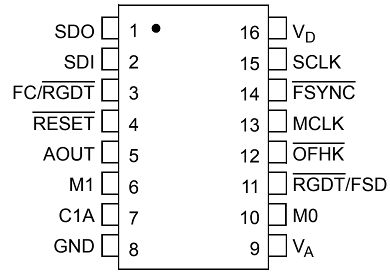


Table 24. Si3021 Pin Descriptions

SOIC Pin #	TSSOP Pin #	Pin Name	Description
1	13	MCLK	**Master Clock Input.** High speed master clock input. Generally supplied by the system crystal clock or modem/DSP.
2	14	$\overline{\text{FSYNC}}$	**Frame Sync Output.** Data framing signal that is used to indicate the start and stop of a communication/data frame.
3	15	SCLK	**Serial Port Bit Clock Output.** Controls the serial data on SDO and latches the data on SDI.
4	16	V_D	**Digital Supply Voltage.** Provides the digital supply voltage to the Si3021, nominally either 5 V or 3.3 V.
5	1	SDO	**Serial Port Data Output.** Serial communication data that is provided by the Si3021 to the modem/DSP.
6	2	SDI	**Serial Port Data Input.** Serial communication and control data that is generated by the modem/DSP and presented as an input to the Si3021.
7	3	FC/$\overline{\text{RGDT}}$	**Secondary Transfer Request Input/Ring Detect Output.** An optional signal to instruct the Si3021 that control data is being requested in a secondary frame. When daisy chain is enabled, this pin becomes the ring detect output. Produces an active low rectified version of the ring signal.
8	4	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si3034 out of sleep mode.
9	5	AOUT	**Analog Speaker Output.** Provides an analog output signal for driving a call progress speaker.

Table 24. Si3021 Pin Descriptions (Continued)

SOIC Pin #	TSSOP Pin #	Pin Name	Description
10	6	M1	**Mode Select 1 Input.** The second of two mode select pins that is used to select the operation of the serial port/DSP interface.
11	7	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1. Used to communicated with the line-side device.
12	8	GND	**Ground.** Connects to the system digital ground.
13	9	V_A	**Analog Supply Voltage.** Provides the analog supply voltage for the Si3021, nominally 5 V. This supply is typically generated internally with an on-chip charge pump set through a control register.
14	10	M0	**Mode Select 0 Input.** The first of two mode select pins that is used to select the operation of the serial port/DSP interface.
15	11	$\overline{\text{RGDT}}$/FSD	**Ring Detect/Delayed Frame Sync Output.** Output signal that indicates the status of a ring signal. Produces an active low rectified version of the ring signal. When daisy chain is enabled, this signal becomes a delayed frame sync to drive a slave device.
16	12	$\overline{\text{OFHK}}$	**Off-Hook Input.** An active low input control signal that provides a termination across TIP and RING for line seizing and pulse dialing.

Pin Descriptions: Si3014

Si3014 (SOIC or TSSOP)

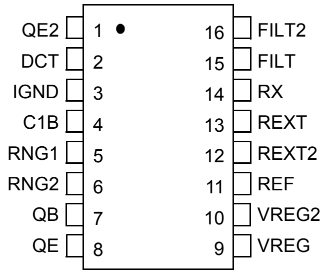


Table 25. 3014 Pin Descriptions

(SOIC or TSSOP) Pin #	Pin Name	Description
1	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	IGND	**Isolated Ground.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1.
5	RNG1	**Ring 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3034.
6	RNG2	**Ring 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3034.
7	QB	**Transistor Base.** Connects to the base of transistor Q3.
8	QE	**Transistor Emitter.** Connects to the emitter of transistor Q3.
9	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**Reference.** Connects to an external resistor to provide a high accuracy reference current.

Table 25. 3014 Pin Descriptions (Continued)

(SOIC or TSSOP) Pin #	Pin Name	Description
12	REXT2	**External Resistor 2.** Sets the complex ac termination impedance.
13	REXT	**External Resistor.** Sets the real ac termination impedance.
14	RX	**Receive Input.** Serves as the receive side input from the telephone network.
15	FILT	**Filter.** Provides filtering for the dc termination circuits.
16	FILT2	**Filter 2.** Provides filtering for the bias circuits.

Ordering Guide

Table 26. Ordering Guide

Chipset	Region	Interface	Digital (SOIC)	Line (SOIC)	Digital (TSSOP)	Line (TSSOP)	Temperature
Si3034	Global	DSP Serial I/F	Si3021-KS	Si3014-KS	Si3021-KT	Si3014-KT	0°C to 70°C
Si3035	FCC/Japan	DSP Serial I/F	Si3021-KS	Si3012-KS	Si3021-KT	Si3012-KT	0°C to 70°C
Si3036	FCC/Japan	AC Link	Si3024-KS	Si3012-KS	Si3024-KT	Si3012-KT	0°C to 70°C
Si3038	Global	AC Link	Si3024-KS	Si3014-KS	Si3024-KT	Si3014-KT	0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-KS	Si3015-KS			0°C to 70°C
Si3044	Enhanced Global	DSP Serial I/F	Si3021-BS	Si3015-BS			–40°C to 85°C
Si3046	FCC/JATE	AC Link	Si3025-KS	Si3012-KS			0°C to 70°C
Si3048	Global	AC Link	Si3025-KS	Si3014-KS			0°C to 70°C

SOIC Outline

Figure 36 illustrates the package details for the Si3021 and Si3014. Table 27 lists the values for the dimensions shown in the illustration.

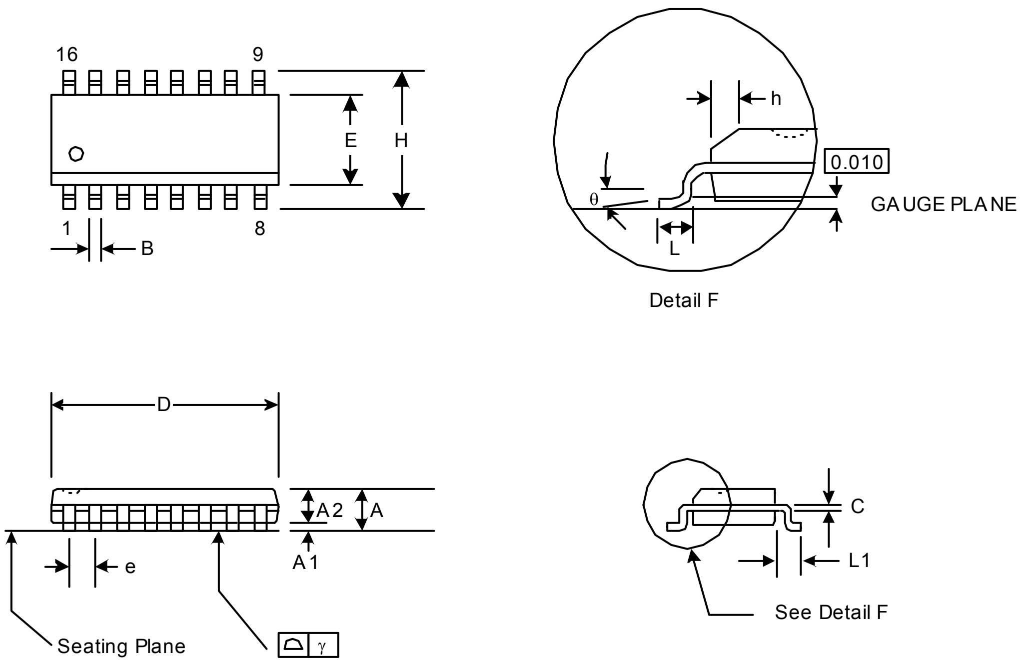


Figure 36. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 27. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
A2	1.30	1.50
B	.33	.51
C	.19	.25
D	9.80	10.01
E	3.80	4.00
e	1.27 BSC	—
H	5.80	6.20
h	.25	.50
L	.40	1.27
L1	1.07BSC	—
γ	—	0.10
θ	0º	8º

TSSOP Outline

Figure 37 illustrates the package details for the Si3021 and Si3014. Table 28 lists the values for the dimensions shown in the illustration.

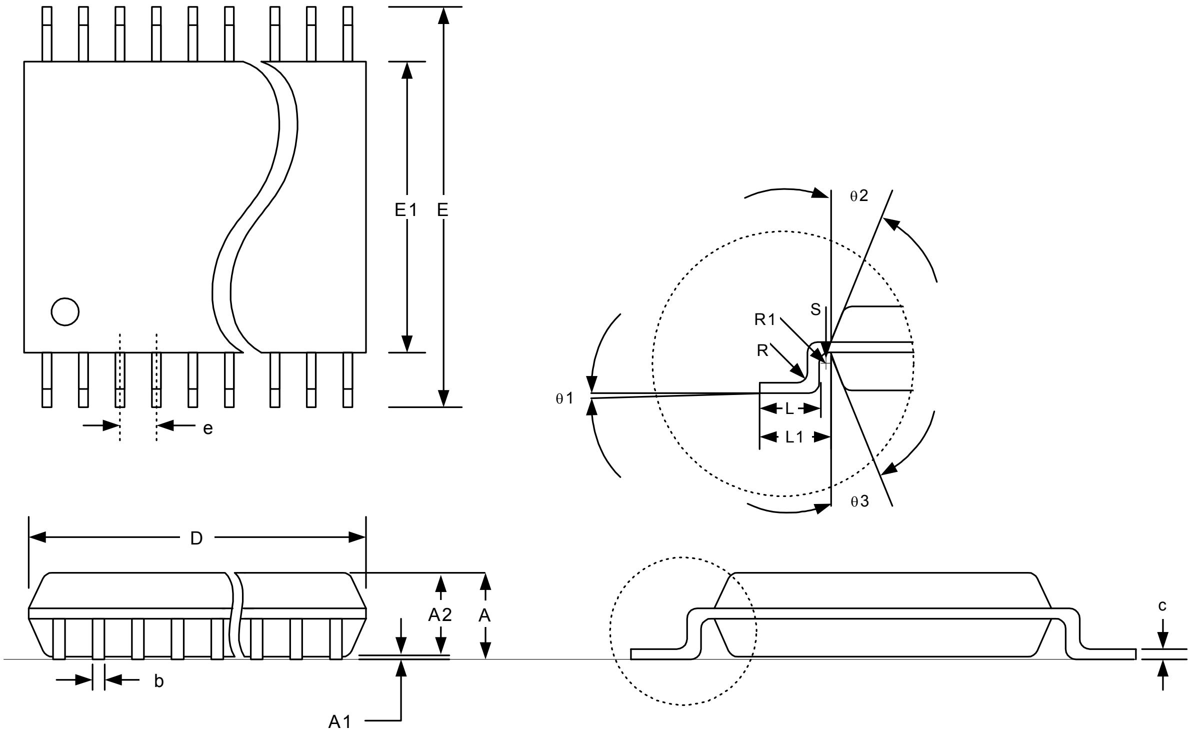


Figure 37. 16-pin Thin Small Shrink Outline Package (TSSOP)

Table 28. Package Diagram Dimensions

Symbol	Millimeters		
	Min	**Nom**	**Max**
A	—	1.10	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.85	5.00	5.15
e	0.65 BSC		
E	6.40 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0	—	8
θ2	12 REF		
θ3	12 REF		

Rev 1.0 to Rev 1.1 Change List

- Typical Application Circuit was updated.
- C24, C25 value changed from 470 pF to 1000 pF and C31, C32 were added in Table 13 and Table 14. In Table 14, the tolerance was also changed from 20% to 10%.
- Power Supply Voltage, Analog maximum changed from 4.75 V to 5.00 V in Table 4.
- Last paragraph updated in “Power Management” text section.

Rev 1.1 to Rev 1.2 Change List

- Added TSSOP pinout and package drawing.
- Added note to Table 2.
- Amended numbers in Table 3.
- Amended numbers in Table 4.
- Amended note #4 in Table 5.
- Amended numbers in Table 7.
- Replaced Figure 4.
- Updated Analog Output text.
- Added China to Table 16.
- Added “On-Chip Charge Pump” section.
- Added “DC Termination Considerations” section.
- Figure 16, “Typical Application Circuit for the Dual Design Si3034 and Si3035,” on page 15 updated.
- Table 13, “Global Component Values,” on page 16 (BOM) updated.
- Table 14, “FCC Component Values—Si3035 Chipset,” on page 17 (BOM) updated.

Rev 1.2 to Rev 2.0 Change List

- Updated schematic and BOM.
- Added Appendix B.
- Corrected transmit frequency response specification to 0 Hz typical.
- Updated “Overload Detection” section text concerning CTR21 mode.
- Removed CTRO bit (Register 19, bit 7).

Rev 2.0 to Rev 2.01 Change List

- Table 16 updated.
- “Appendix B—CISPR22 Compliance” updated.
- The “Ringer Impedance Network” figure and the “Component Values—Optional Ringer Impedance Network” table were deleted from the “Ringer Impedance” section as well as a paragraph discussing Czech Republic designs.
- The “Dongle Applications Circuit” figure was deleted.

NOTES:

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